Avnet® Mini-Module Plus Baseboard 2 User Guide

Version 1.2

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Prior Version History

Version	Date	Comment
Rev B V1.0	4/27/2012	Initial release for production board (AES-MMP-BB2-G Revision B)
Rev C V1.0	10/22/2012	Added section 2.11 for 12V fan connector. Addresses Rev B and Rev C baseboards.
Rev C V1.1	9/5/2013	Corrected table 14 for FMC1-LA10_P/N pin connections
Rev C V1.2	1/1/2015	Added clarification and illustrations for removal of SW13 and SW14 in Section 2.10

Contents

Figures

Tables

Introduction

The purpose of this manual is to describe the functionality and contents of the Avnet Mini-Module Plus Baseboard 2 from Avnet Electronics Marketing. This document includes instructions for operating the board and descriptions of the hardware features.

1.1 Description

The Avnet Mini-Module Plus Baseboard 2 provides a complete hardware environment for designers to accelerate their time to market. The kit delivers a stable platform to develop and test designs targeted to the advanced Xilinx FPGA families. The new and improved Mini-Module Baseboard 2 design features a smaller form factor than the original Mini-Module Baseboard and supports the Xilinx Kintex-7 series family of FPGAs while maintaining backward compatibility with the Xilinx Virtex-5 FXT family Mini-Module. The Avnet Mini-Module Plus Baseboard 2 offers a prototyping environment to effectively demonstrate the enhanced benefits of leading edge Xilinx FPGA solutions. Reference designs are provided on Avnet's Design Resource Center (DRC) website to exercise standard peripherals on the evaluation board for a quick start to device familiarization.

The Avnet Mini-Module Plus Baseboard 2 as a complete system consists of three components, the Mini Module Plus Baseboard 2, the Kintex-7 Mini Module Plus, and the user's choice of a Power Module. Modular power supply design allows users to use different manufacturer's power solution on the Mini Module Plus Baseboard 2. Refer to the Power section 2.10 of this document for more information about the power modules that Avnet provides for baseboard.

1.2 Board Features

- **Xilinx FPGA Mini-Modules Supported**
  - Xilinx Kintex-7 AES-MMP-7K325T-G
  - Xilinx Virtex-5 AES-MMP-V5FXT30-G
  - Xilinx Virtex-5 AES-MMP-V5FXT70-G
  - Artix-7 Mini-Module
  - Zynq Mini-Module
- **I/O Connectors**
  - One Mini Module Plus Slot
  - One FMC LPC Slot (2.5V or 3.3V VADJ)
  - DisplayPort Output
  - Two PMOD Headers
- **GTX Transceiver Connectors**
  - One Small-Form Pluggable (SFP) cage
  - One supplied on an FMC connectors for use by an expansion module
  - One PCI Express x4 add-in card interface
    - 4-lanes @ 5.0 Gbps with Kintex-7 Mini-Module (PCI Express 2.0)
    - 4-lanes @ 2.5 Gbps with Virtex-5 Mini-Module (PCI Express)
  - One via SMA Connectors
  - One DisplayPort Connector (TX Only)
- **Memory**
  - Micro SD Card Interface
- **Communication**
  - USB-RS232 Port
- **Clocks**
  - Programmable LVDS Clock Source (MGT reference clock input)
  - Programmable LVCMOS Clock Source

- **User I/O**
  - 5-User LEDs
  - 8-position DIP Switch
  - 4-User Push Button Switches
- **Power**
  - Regulated 1.35V/1.5V, 1.8V, 2.0V, 3.3V, 1.0V, 2.5V, 1.0V_MGT and 1.2V_MGT supply voltages derived from an external 12 V supply.
- **Configuration**
  - Digilent JTAG-SMT1 Module
  - PC4 JTAG Header

1.3 Test Files

The configuration PROM on both Kintex-7 and Virtex-5 Mini-Modules come programmed with a factory test example design. The factory test can be used to verify the functionality of the peripherals on the board can be found on the Avnet Electronics Marketing Design Resource Center (DRC) web site. Some of the factory tests require additional cabling that is not supplied with the Mini-Module boards.

The test files for each Mini-Module will be located on the Mini-Module web pages respectively. Below are the links to each Mini-Module's web page on the DRC:

Kintex-7 Mini-Module
http://avnet.com/us/design/drc/Pages/Xilinx-Kintex-7-Mini-Module-Plus.aspx

Virtex-5 FXT Mini-Module
http://avnet.com/us/design/drc/Pages/Xilinx-Virtex-5-FXT-Mini-Module-Plus.aspx

1.4 Reference Designs

Reference designs that demonstrate some of the potential applications of the Mini-Module Plus Baseboard 2 can be downloaded from the Avnet Design Resource Center. The reference designs include all of the source code and project files necessary to implement the designs. See the PDF document included with each reference design for a complete description of the design and detailed instructions for running a demonstration on the development board. Check the DRC periodically for updates and new designs.

Kintex-7 Mini-Module
http://avnet.com/us/design/drc/Pages/Xilinx-Kintex-7-Mini-Module-Plus.aspx

Virtex-5 FXT Mini-Module
http://avnet.com/us/design/drc/Pages/Xilinx-Virtex-5-FXT-Mini-Module-Plus.aspx

Figure 1 – Mini-Module Plus Baseboard 2 Picture

1.5 Ordering Information

The following table lists the Avnet Mini-Module Plus Baseboard 2 part number and available Mini-Module hardware options. Internet link at http://avnet.com/us/design/drc/Pages/Xilinx-Kintex-7-Mini-Module-Plus.aspx

Table 1 - Ordering Information

	Part Number	Hardware
Baseboard	AES-MMP-BB2-G	Avnet Mini-Module Plus baseboard 2
Mini-Module Hardware Options	AES-MMP-7K325T-G	Xilinx Kintex-7 FXT Mini-Module Plus populated with XC7K325T-1FFG676 FPGA
	AES-MMP-7K410T-G	Xilinx Kintex-7 FXT Mini-Module Plus populated with XC7K410T-1FFG676 FPGA
	AES-MMP-V5FXT70-G	Xilinx Virtex-5 FXT Mini-Module Plus populated with XC5VFX70T-2FF665 FPGA
	AES-MMP-V5FXT30-G	Xilinx Virtex-5 FXT Mini-Module Plus populated with XC5VFX30T-2FF665 FPGA
Power Module Hardware Options	AES-POM-TIS1-G	Texas Instruments Power Module
	AES-POM-TISN-G	Texas instruments Simple Switcher Power Module
	AES-POM-MXM1-G	Maxim Power Module
	AES-POM-ANA1-G	Analog Devices Power Module
	AES-POM-LTM1-G	GE Energy Power Module

2 Functional Description

A high-level block diagram of the Avnet Mini-Module Plus Baseboard 2 is shown below followed by a brief description of each sub-section.

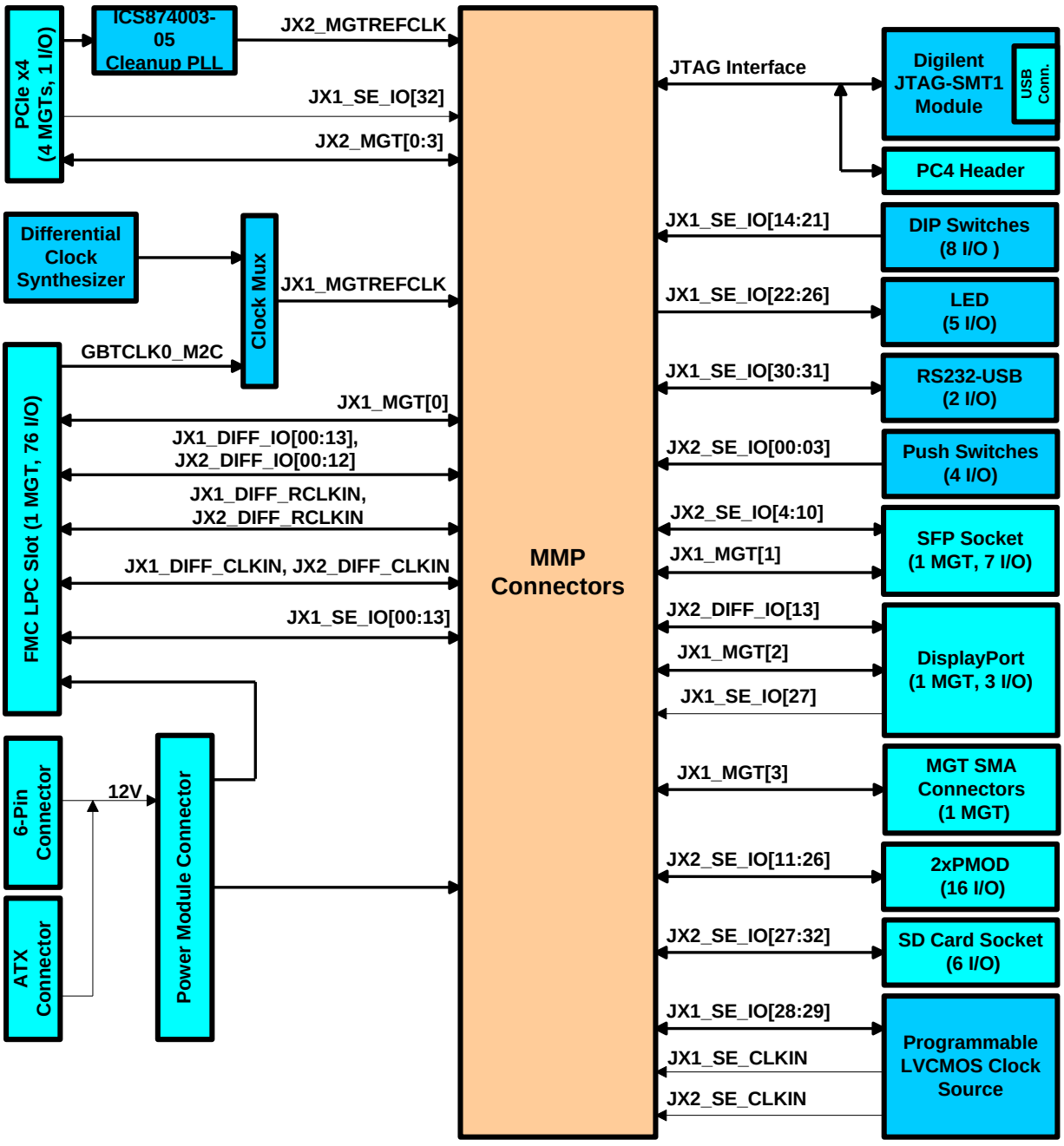


Figure 2 - Avnet Mini-Module Plus Baseboard 2 Block Diagram

2.1 GTX (Gigabit Transceiver) Interfaces

The Mini-Module Plus Baseboard 2 supports a variety of Gigabit transceiver interfaces. GTX Transceivers are full-duplex serial transceivers for point-to-point transmission applications. The number of transceivers available is dependent on the model of Mini-Module that is installed on the baseboard. Refer to the Mini-Module's User Guide to get details on the number of transceivers available and performance details for a specific model of Mini-Module. The table below lists a sub-set of communication protocols supported by the Virtex-5 and Kintex-7 Mini-Modules.

Table 2 - Communications Standards

Standards	I/O Bit Rate (Gb/s)
PCI Express	2.5
PCI Express 2.0	5.0
SFI-5	2.488 – 3.125
OC-12	0.622
OC-48	2.488
Fibre Channel	1.06
	2.12
Gigabit Ethernet	1.25
10-Gbit Fibre Channel	3.1875
Infiniband	2.5
HD-SDI	1.485
	1.4835
	3.0
Serial Rapid I/O	1.25
	2.5
	3.125
Aurora (Xilinx protocol)	0.100 – 3.75

The Mini-Module Plus Baseboard 2 implements the following GTX interfaces:

Table 3 - GTX Interfaces Supported

GTX Interface	Lanes
SMA	x1
SFP	x1
FMC	x1
PCI Express	x4
DisplayPort	x1 (TX only)

2.1.1 GTX Reference Clock Inputs

GTX interfaces require a reference clock to operate. The Mini-Module Plus Baseboard 2 offers three sources for the GTX reference clocks.

A single programmable LVDS synthesizer (CDCM61001) is used to provide a variable clock source to the dedicated GTX clock inputs. The CDCM61001 is programmed by setting dip switches SW1 and SW2 on the board. The CDCM 61001 uses a 27MHz reference clock. The synthesizer provides reference clock frequencies that support the full range of line rates. The programmable LVDS clock source is routed through a 2:1 MUX, and is shared by the FMC slot's gigabit clock. The diagram below shows the architecture of these two GTX clock sources.

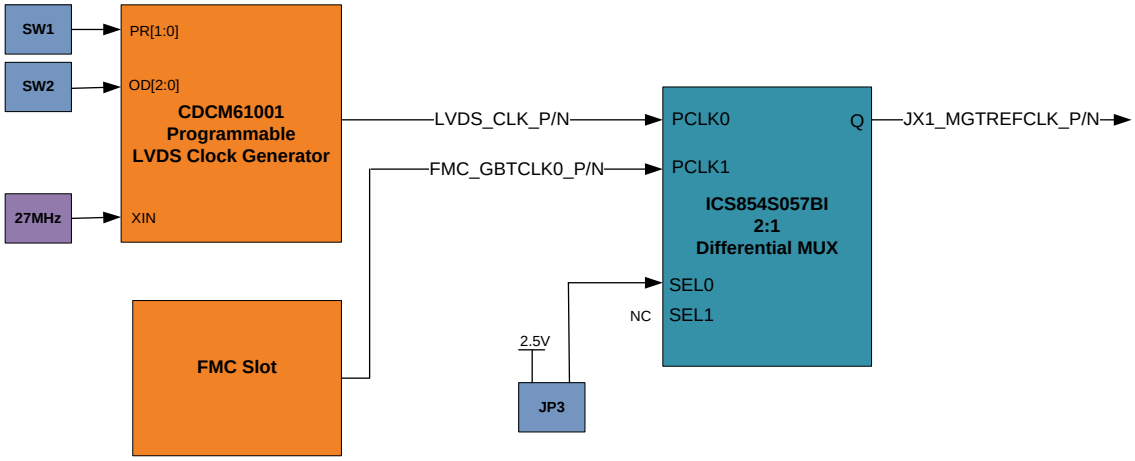


Figure 3 – GTX Reference Clock Sources

Placing a jumper shunt on JP3 will enable the MUX to pass the FMC_GBTCLK0 pair to the JX1_MGTREFCLK pins on the Mini-Module Plus mating connectors. The default configuration from the factory is no jumper placed, passing the clock generator's signal pair through to the connector JX1.

The table below shows the electrical connections of the JX1_MGTREFCLK pair to the Mini-Module Plus mating connector JX1.

Table 4 – JX1 GTX Reference Clock Pin Assignments

Signal Name	Mini-Module Plus mating Connector (JX1)
JX1_MGTREFCLK_P	JX1.67
JX1_MGTREFCLK_N	JX1.69

PCI Express applications use the 100 MHz reference clock provided over the card edge. The following figure shows the PCI Express reference clock architecture.

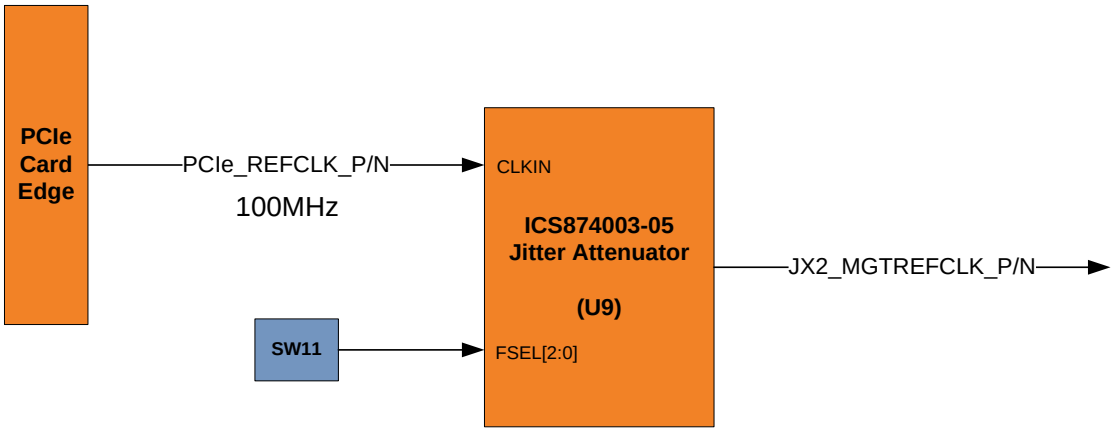


Figure 4- PCI Express Reference Clock

The ICS874003 device can provide a 250MHz, 125MHz, or a 100MHz output by configuring the dip switch SW11.

The table below shows the appropriate dip switch settings for the valid output frequencies.

Table 5 – PCI Express Reference Clock Frequencies

SW11[3:0]	Output Frequency
x000	250MHz
x010	125MHz
x101	100MHz

The table below shows the electrical connections of the JX2_MGTREFCLK pair to the Mini-Module Plus mating connector JX2.

Table 6 – PCI Express reference Clock Pin Assignments

Signal Name	Mini-Module Plus mating Connector JX2)
JX2_MGTREFCLK_P	JX2.67
JX2_MGTREFCLK_N	JX2.69

2.1.2 PCI Express x4 Add-in Card

The PCI Express electrical interface on the Mini-Module Plus Baseboard 2 development board consists of 4 lanes, each lane having a unidirectional transmit and receive differential pair. Each lane supports both first generation data rate of 2.5 Gbps and PCI Express 2.0 data rate of 5.0Gbps. In addition to the 4 serial lanes there is a 100MHz reference clock that is provided from the system slot. In order to work in open systems, add-in cards must use the reference clock provided over the PCI Express card edge to be frequency locked with the host system.

To add clocking integrity and flexibility in the end user design the Mini-Module Plus Baseboard 2 development board utilizes the on board ICS874003-05 jitter attenuator. This device provides a stable, low jitter reference clock that is programmable. See the figure below for an illustration of how the PCI Express reference clock is connected to the target FPGA.

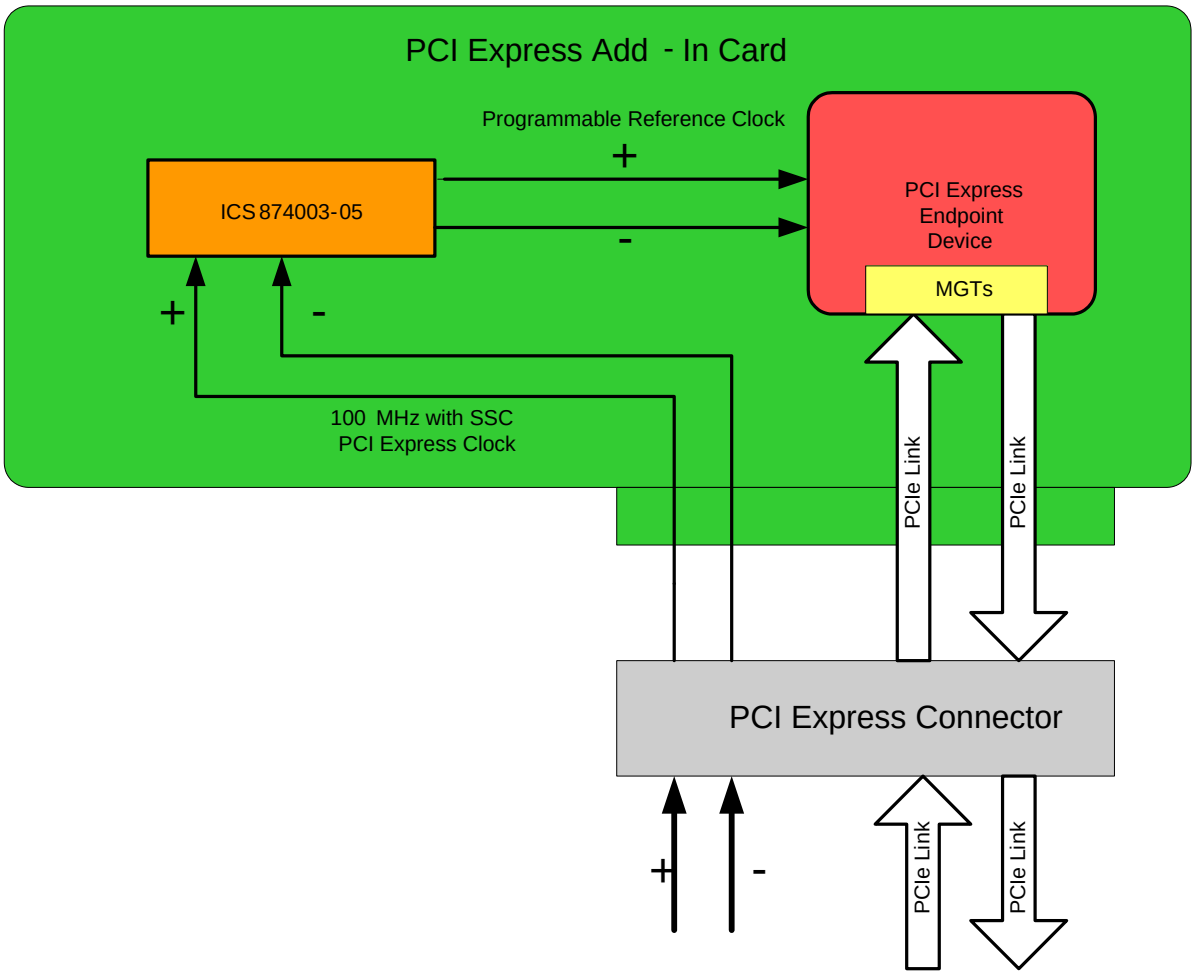


Figure 5 - PCI Express Electrical Interface

See **Section 2.1.1** for details about PCI Express programmable reference clock.

There is also a side band signal from the PCI Express card edge that connects to a regular I/O pin on the target endpoint device. The “PERST#” signal is an active low reset signal provided by the host PCI Express slot.

The lane width of the PCI Express interface is determined by the PRSNT1# and PRSNT2# connections. There are separate PRSNT2# pins for each of the lane options: one lane (x1) and four lanes (x4). These pins are pulled-up on the host motherboard. There is a single PRSNT1# pin that is pulled-low or tied to GND on the host motherboard. The add-in card connects the PRSNT1# pin to the PRSNT2# pin for the widest lane option in most applications, which effectively pulls the corresponding PRSNT2# pin low. This indicates to the host controller the lane width supported by the add-in card. The Mini-Module Plus Baseboard 2 development board provides the ability for the user to select the lane width by connecting the desired PRSNT2# pin with a jumper on JP5. See the figure below for an illustration of JP5

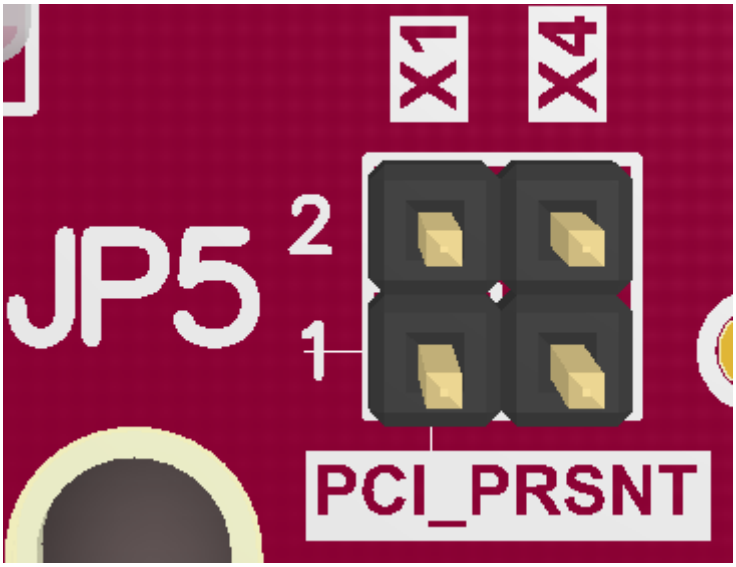


Figure 6 – PCI_PRSNT Configuration Jumper

Placing a jumper shunt across JP5 positions 1-2 indicates to the host system a x1 interface and placing a jumper shunt across JP positions 3-4 indicates a x4 interface.

The PCI Express receive lanes are AC coupled (DC blocking capacitors are included in the signal path) on the development board as required by the PCI Express specification. The Transmit pairs are AC coupled on the Mini-Module that is installed on the baseboard.

The table below shows the electrical connections to the Mini-Module Plus mating connector JX2.

Table 7 - PCI Express JX2 Pin Assignments

Signal Name	Mini-Module Plus mating Connector (JX2)
PCIe_RX0P	JX2.55
PCIe_RX0N	JX2.57
PCIe_TX0P	JX2.56
PCIe_TX0N	JX2.58
PCIe_RX1P	JX2.61
PCIe_RX1N	JX2.63
PCIe_TX1P	JX2.62
PCIe_TX1N	JX2.64
PCIe_RX2P	JX2.43
PCIe_RX2N	JX2.45
PCIe_TX2P	JX2.44
PCIe_TX2N	JX2.46
PCIe_RX3P	JX2.49
PCIe_RX3N	JX2.51
PCIe_TX3P	JX2.50
PCIe_TX3N	JX2.52

2.1.3 SFP Connector

The Mini-Module Plus Baseboard 2 provides for a Small Form-factor Pluggable (SFP) interface which provides the ability to support optical links with the addition of optical transceiver modules (not included in the kit). The following figure shows a high-level block diagram of the SFP interface on the development board. This interface utilizes one GTX channel and a set of low-speed control signals to interface to the SFP module. The programmable LVDS synthesizer on the board is used to provide the reference clock. The SFP interface on the Mini-Module Plus Baseboard 2 development board has been designed to support transceivers with transmission rates up to 3.75 Gbps operating over multimode or single mode fiber.

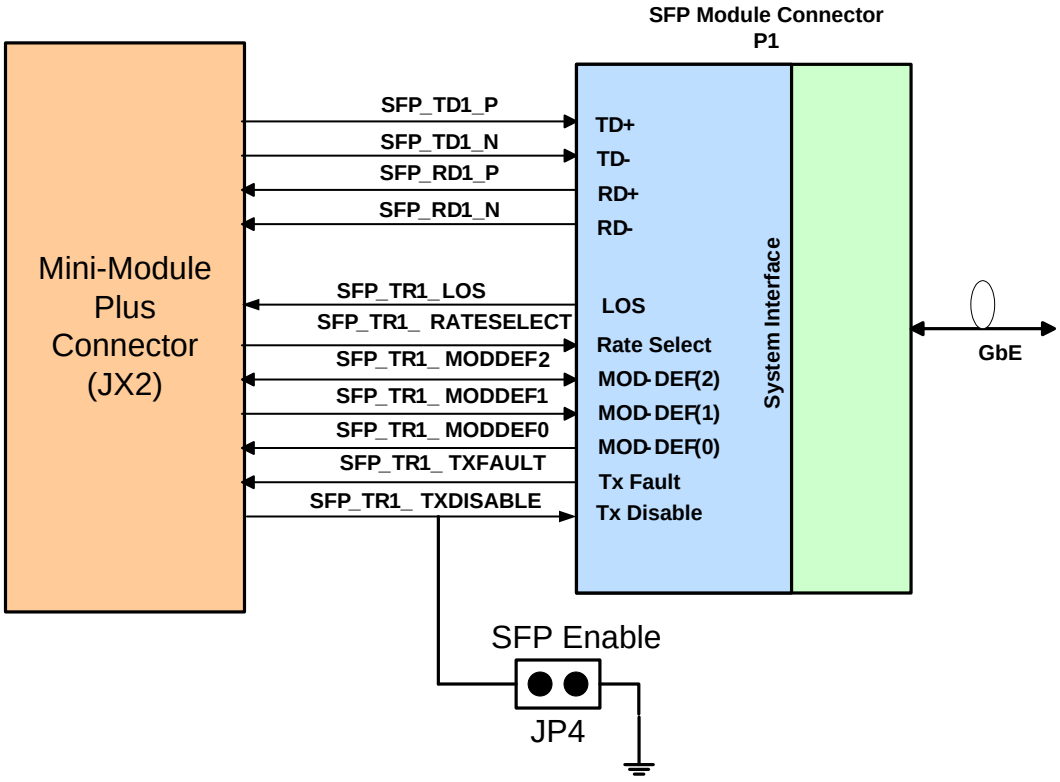


Figure 7 - SFP Module Interface

The SFP connector includes a Host Board Connector, and top and bottom EMI cage. The Host Connector is directly connected or DC coupled to the GTX port. SFP compliant modules include AC coupling capacitors in the modules for both transmit and receive signal paths so the AC coupling internal to the target GTX receiver may be bypassed.

The table below shows the electrical connections to the Mini-Module Plus mating connector JX2.

Table 8 - SFP JX1/JX2 Pin Assignments

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
SFP0_RXP	JX1.49
SFP0_RXN	JX1.51
SFP0_TXP	JX1.50
SFP0_TXN	JX1.52
SFP_LOS	JX2.15
SFP_RATESEL	JX2.12
SFP_MODE0	JX2.11
SFP_MODE1	JX2.10
SFP_MODE2	JX2.9
SFP_TXFAULT	JX2.7
SFP_TXDISABLE	JX2.8

SFP modules connect to the board via the Host Board Connector defined in the SFP Multi-Source Agreement (MSA). This 20-pin connector provides connections for power, ground, high-speed serial data, and the low-speed control signals for controlling the operation of the SFP module. The following figure shows the host connector used on the Mini-Module Plus Baseboard 2.

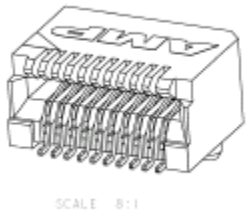


Figure 8 - Host Board Connector AMP 1367073-1
(photo taken from AMP Web Page)

The following table lists the Host Board Connector pin assignments and provides a brief description of each signal.

Table 9 - SFP Host Connector Pin Description

Pin Number	Signal Name	Function
1	VEET	Transmitter Ground
2	Tx Fault	Transmitter Fault Indication
3	Tx Disable	Transmitter Disable
4	MOD-DEF(2)	Module Definition 2 (Serial Interface Data Line)
5	MOD-DEF(1)	Module Definition 1 (Serial Interface Clock Line)
6	MOD-DEF(0)	Module Definition 0 (Module Present Signals, active low)
7	Rate Select	Not Connected
8	LOS	Loss of Signal
9	VEER	Receiver Ground
10	VEER	Receiver Ground
11	VEER	Receiver Ground
12	RD-	Inverse Received Data Out
13	RD+	Received Data Out
14	VEER	Receiver Ground
15	VCCR	Receiver Power
16	VCCT	Transmitter Power
17	VEET	Transmitter Ground
18	TD+	Transmitter Data In
19	TD-	Inverse Transmitter Data In
20	VEET	Transmitter Ground

2.1.4 GTX on FMC Expansion Connectors JX1 AND JX2

One GTX channel is interfaced to the target Mini-Module via the FMC slot JX3. Should a user want to connect an FMC daughter board to the Mini-Module Plus Baseboard 2 one gigabit channel is supported. The GTX channel is not AC coupled on the baseboard. The user must evaluate whether AC coupling is required on the daughter card to safely interface with the target Mini-Module.

Table 10 - FMC GTX JX1 Pin Assignments

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
FMC1_DP0_C2M_P	JX1.44
FMC1_DP0_C2M_N	JX1.46
FMC1_DP0_M2C_P	JX1.43
FMC1_DP0_M2C_N	JX1.45

2.1.5 SMA

One GTX channel is interfaced to the target Mini-Module via the on-board SMA connectors. The SMA connectors are referenced on the board as J11, J12, J13 and J14.

Table 11 - SMA GTX JX1 Pin Assignments

Signal Name	Mini-Module Plus mating Connector (JX1)
SMA_TXP	JX1.62
SMA_TXN	JX1.64
SMA_RXP	JX1.61
SMA_RXN	JX1.63

2.1.6 DisplayPort

One half of a GTX channel (transmit only) is interfaced to the target Mini-Module via the DisplayPort connector J9. This is a transmit only port that will allow the user to transmit DisplayPort data to the DisplayPort capable video monitor. The DisplayPort interface also utilizes one low speed differential auxiliary channel and a single DisplayPort HPD (Hot Plug Detect) single ended I/O signal.

Table 12 – DisplayPort JX1/JX2 Pin Assignments

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
DP_ML_L0_P	JX1.56
DP_ML_L0_N	JX1.58
DP_AUX_CH_P	JX2.112
DP_AUX_CH_N	JX2.114
DP_HPD	JX1.32

2.2 FMC Low Pin Count (LPC) Interface

The FMC specification defines the LPC interface to be a 160-pin connector arranged in a 4x40 array. The LPC connector is populates 160 of the 400 possible positions. The HPC (High Pin Count) version of the connector has all positions populated.

The FMC LPC configuration implemented on the Mini-Module Plus Baseboard 2 development board uses one LPC connector (SAMTEC part number ASP-134603-01), for a total of 68 user I/Os. The connector is referenced as JX3 on the board.

The FMC specification defines five user signal types: Differential I/O, Differential Clock Inputs, Differential Clock Outputs, MGT I/O, and MGT Clock Inputs. Because the FPGA I/Os can be configured for either single-ended or differential use, the differential I/Os defined in the FMC specification can serve a dual role. All the differential I/O signals can be configured as either differential pairs or single-ended signals, as required by the end application. In providing differential signaling, higher performance LVDS interfaces can be implemented between the Mini-Module Plus Baseboard 2 development board and an FMC LPC module. Connection to high speed A/Ds, D/As, and flat panel displays are possible with this signaling configuration. Applications that require

single-ended signals only can use each differential pair as two single-ended signals, for a total of 68 single-ended I/O per LPC connector.

Table 13 - FMC LPC Connector Signals

Signal Names	Signal Description	Pins per Connector
FMC_LA**_P/N	34 Differential I/O Pairs	68
Total	**User I/O**	**68**
FMC_CLK0_C2M_P/N	1 Differential Clock Pair (Carrier to Mezzanine)	2
FMC_CLK0_M2C_P/N	1 Differential Clock Pair (Mezzanine to Carrier)	2
Total	**Clock I/O**	**4**
FMC_DP0_M2C_P/N	1 MGT Receive Differential Data Pair	2
FMC_DP0_C2M_P/N	1 MGT Transmit Differential Data Pair	2
FMC_GBTCLK0_M2C_P/N	1 MGT Differential Clock Pair	2
Total	**MGT I/O**	**6**

	H	G	D	C
1	VREF_A_M2C	GND	PG_C2M	GND
2	PRSNT_M2C_L	CLK1_M2C_P	GND	DP0_C2M_P
3	GND	CLK1_M2C_N	GND	DP0_C2M_N
4	CLK0_M2C_P	GND	GBTCLK0_M2C_P	GND
5	CLK0_M2C_N	GND	GBTCLK0_M2C_N	GND
6	GND	LA00_P_CC	GND	DP0_M2C_P
7	LA02_P	LA00_N_CC	GND	DP0_M2C_N
8	LA02_N	GND	LA01_P_CC	GND
9	GND	LA03_P	LA01_N_CC	GND
10	LA04_P	LA03_N	GND	LA06_P
11	LA04_N	GND	LA05_P	LA06_N
12	GND	LA08_P	LA05_N	GND
13	LA07_P	LA08_N	GND	GND
14	LA07_N	GND	LA09_P	LA10_P
15	GND	LA12_P	LA09_N	LA10_N
16	LA11_P	LA12_N	GND	GND
17	LA11_N	GND	LA13_P	GND
18	GND	LA16_P	LA13_N	LA14_P
19	LA15_P	LA16_N	GND	LA14_N
20	LA15_N	GND	LA17_P_CC	GND
21	GND	LA20_P	LA17_N_CC	GND
22	LA19_P	LA20_N	GND	LA18_P_CC
23	LA19_N	GND	LA23_P	LA18_N_CC
24	GND	LA22_P	LA23_N	GND
25	LA21_P	LA22_N	GND	GND
26	LA21_N	GND	LA26_P	LA27_P
27	GND	LA25_P	LA26_N	LA27_N
28	LA24_P	LA25_N	GND	GND
29	LA24_N	GND	TCK	GND
30	GND	LA29_P	TDI	SCL
31	LA28_P	LA29_N	TDO	SDA
32	LA28_N	GND	3P3VAUX	GND
33	GND	LA31_P	TMS	GND
34	LA30_P	LA31_N	TRST_L	GA0
35	LA30_N	GND	GA1	12P0V
36	GND	LA33_P	3P3V	GND
37	LA32_P	LA33_N	GND	12P0V
38	LA32_N	GND	3P3V	GND
39	GND	VADJ	GND	3P3V
40	VADJ	GND	3P3V	GND
	LPC Connector	LPC Connector	LPC Connector	LPC Connector

Figure 9 - FMC LPC Connector Pin Out

Note: For the FMC LPC, the connector columns K, J, F, E, B, and A are not used and not shown in the above table.

The SAMTEC connector plug on the board (CC-LPC-10 part number: ASP-134603-01) mates with the SAMTEC low pin count receptacle (MC-LPC-10 part number: ASP-134604-01), located on FMC modules.

Since the FMC connectors are connected to the I2C bus a geographical address must be given to the connector. The GA[1:0] inputs provide a means to give the connector an I2C address. For JX3 the address is hard wired to 0x00 by tying these inputs low through pull-down resistors.

The following diagram and table shows how FMC LPC connector JX3 is connected to the Mini-Module Plus mating connectors JX1 and JX2.

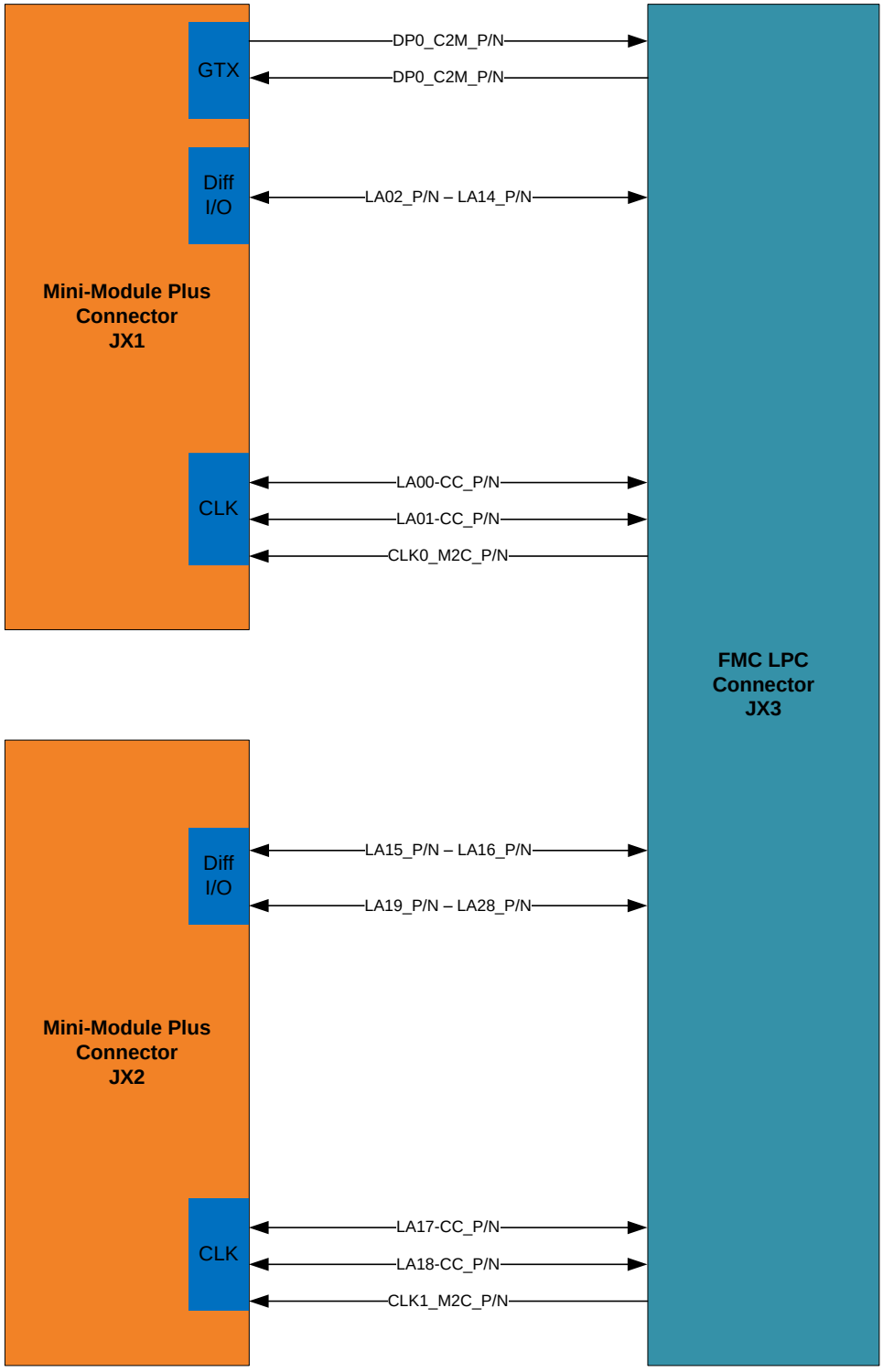


Figure 10 - FMC LPC Connector JX3 Block Diagram

Table 14 - FMC LPC Connector JX1 Pin Assignments

Mini-Module Plus mating Connector (JX1/JX2)	Schematic Net Name	FMC Connector Pin Location (JX1)	FMC Connector Symbol Name
-	GND	C1	GND
JX1.44	**FMC1_DP0_C2M_P**	**C2**	**DP0_C2M_P**
JX1.46	**FMC1_DP0_C2M_N**	**C3**	**DP0_C2M_N**
-	GND	C4	GND
-	GND	C5	GND
JX1.43	**FMC1_DP0_M2C_P**	**C6**	**DP0_M2C_P**
JX1.45	**FMC1_DP0_M2C_N**	**C7**	**DP0_M2C_N**
-	GND	C8	GND
-	GND	C9	GND
JX1.88	**FMC1_LA06_P**	**C10**	**LA06_P**
JX1.90	**FMC1_LA06_N**	**C11**	**LA06_N**
-	GND	C12	GND
-	GND	C13	GND
JX1.105	**FMC1_LA10_P**	C14	LA10_P
JX1.107	**FMC1_LA10_N**	C15	LA10_N
-	GND	C16	GND
-	GND	C17	GND
JX1.111	**FMC1_LA14_P**	**C18**	**LA14_P**
JX1.113	**FMC1_LA14_N**	**C19**	**LA14_N**
-	GND	C20	GND
-	GND	C21	GND
JX2.81	**FMC1_LA18_CC_P**	**C22**	**LA18_P_CC**
JX2.83	**FMC1_LA18_CC_N**	**C23**	**LA18_N_CC**
-	GND	C24	GND
-	GND	C25	GND
JX2.106	**FMC1_LA27_P**	**C26**	**LA27_P**
JX2.108	**FMC1_LA27_N**	**C27**	**LA27_N**
-	GND	C28	GND
-	GND	C29	GND
JX1.14	**SCL_0**	**C30**	**SCL**
JX1.13	**SDA_0_VT**	**C31**	**SDA**
-	GND	C32	GND
-	GND	C33	GND
-	**PULL-DOWN**	**C34**	**GA0**
-	12V	C35	12P0V
-	-	C36	GND
-	12V	C37	12P0V
-	-	C38	GND
-	3.3V	C39	3P3V

-	-	C40	GND
-	**FMC_VADJ(PULL-UP)**	**D1**	**PG_C2M**
-	GND	D2	GND
-	GND	D3	GND
JX1.67	**CLK_MUX_OUT_P**	**D4**	**GBTCLK0_M2C_P**
JX1.69	**CLK_MUX_OUT_N**	**D5**	**GBTCLK0_M2C_N**
-	GND	D6	GND
-	GND	D7	GND
JX1.75	**FMC1_LA01_CC_P**	**D8**	**LA01_P_CC**
JX1.77	**FMC1_LA01_CC_N**	**D9**	**LA01_N_CC**
-	GND	D10	GND
JX1.87	**FMC1_LA05_P**	**D11**	**LA05_P**
JX1.89	**FMC1_LA05_N**	**D12**	**LA05_N**
-	GND	D13	GND
JX1.106	**FMC1_LA09_P**	**D14**	**LA09_P**
JX1.108	**FMC1_LA09_N**	**D15**	**LA09_N**
-	GND	D16	GND
JX1.112	**FMC1_LA13_P**	**D17**	**LA13_P**
JX1.114	**FMC1_LA13_N**	**D18**	**LA13_N**
-	GND	D19	GND
JX2.117	**FMC1_LA17_CC_P**	**D20**	**LA17_P_CC**
JX2.119	**FMC1_LA17_CC_N**	**D21**	**LA17_N_CC**
-	GND	D22	GND
JX2.87	**FMC1_LA23_P**	**D23**	**LA23_P**
JX2.89	**FMC1_LA23_N**	**D24**	**LA23_N**
-	GND	D25	GND
JX2.111	**FMC1_LA26_P**	**D26**	**LA26_P**
JX2.113	**FMC1_LA26_N**	**D27**	**LA26_N**
-	GND	D28	GND
JX2.1	**JTAG_TCK**	**D29**	**TCK**
JX1.2	**MMP_TDO**	**D30**	**TDI**
-	**FMC1_TDO**	**D31**	**TDO**
-	FMC_3.3V	D32	3P3VAUX
JX2.2	**JTAG_TMS**	**D33**	**TMS**
JX1.15	**FMC_TRST_L**	**D34**	**TRST_L**
-	**PULLD-DOWN**	**D35**	**GA1**
-	3.3V	D36	3P3V
-	GND	D37	GND
-	3.3V	D38	3P3V
-	GND	D39	GND
-	3.3V	D40	3P3V
-	GND	G1	GND
JX2.118	**FMC1_CLK1_M2C_P**	**G2**	**CLK1_M2C_P**

JX2.120	**FMC1_CLK1_M2C_N**	**G3**	**CLK1_M2C_N**
-	GND	G4	GND
-	GND	G5	GND
JX1.117	**FMC1_LA00_CC_P**	**G6**	**LA00_P_CC**
JX1.119	**FMC1_LA00_CC_N**	**G7**	**LA00_N_CC**
-	GND	G8	GND
JX1.82	**FMC1_LA03_P**	**G9**	**LA03_P**
JX1.84	**FMC1_LA03_N**	**G10**	**LA03_N**
-	GND	G11	GND
JX1.94	**FMC1_LA08_P**	**G12**	**LA08_P**
JX1.96	**FMC1_LA08_N**	**G13**	**LA08_N**
-	GND	G14	GND
JX1.100	**FMC1_LA12_P**	**G15**	**LA12_P**
JX1.102	**FMC1_LA12_N**	**G16**	**LA12_N**
-	GND	G17	GND
JX2.76	**FMC1_LA16_P**	**G18**	**LA16_P**
JX2.78	**FMC1_LA16_N**	**G19**	**LA16_N**
-	GND	G20	GND
JX2.82	**FMC1_LA20_P**	**G21**	**LA20_P**
JX2.84	**FMC1_LA20_N**	**G22**	**LA20_N**
-	GND	G23	GND
JX2.94	**FMC1_LA22_P**	**G24**	**LA22_P**
JX2.96	**FMC1_LA22_N**	**G25**	**LA22_N**
-	GND	G26	GND
JX2.100	**FMC1_LA25_P**	**G27**	**LA25_P**
JX2.102	**FMC1_LA25_N**	**G28**	**LA25_N**
-	GND	G29	GND
JX1.3	**FMC1_LA29_P**	**G30**	**LA29_P**
JX1.4	**FMC1_LA29_N**	**G31**	**LA29_N**
-	GND	G32	GND
JX1.5	**FMC1_LA31_P**	**G33**	**LA31_P**
JX1.6	**FMC1_LA31_N**	**G34**	**LA31_N**
-	GND	G35	GND
JX1.9	**FMC1_LA33_P**	**G36**	**LA33_P**
JX1.10	**FMC1_LA33_N**	**G37**	**LA33_N**
-	GND	G38	GND
-	FMC_VADJ	G39	VADJ_2.5V
-	GND	G40	GND
-	-	H1	VREF_A_M2C
JX1.16	**FMC1_PRSNT_M2C_L_VT**	**H2**	**PRSNT_M2C_L**
-	GND	H3	GND
JX1.118	**FMC1_CLK0_M2C_P**	**H4**	**CLK0_M2C_P**
JX1.120	**FMC1_CLK0_M2C_N**	**H5**	**CLK0_M2C_N**

-	GND	H6	GND
JX1.76	**FMC1_LA02_P**	**H7**	**LA02_P**
JX1.78	**FMC1_LA02_N**	**H8**	**LA02_N**
-	GND	H9	GND
JX1.81	**FMC1_LA04_P**	**H10**	**LA04_P**
JX1.83	**FMC1_LA04_N**	**H11**	**LA04_N**
-	GND	H12	GND
JX1.93	**FMC1_LA07_P**	**H13**	**LA07_P**
JX1.95	**FMC1_LA07_N**	**H14**	**LA07_N**
-	GND	H15	GND
JX1.99	**FMC1_LA11_P**	**H16**	**LA11_P**
JX1.101	**FMC1_LA11_N**	**H17**	**LA11_N**
-	GND	H18	GND
JX2.75	**FMC1_LA15_P**	**H19**	**LA15_P**
JX2.77	**FMC1_LA15_N**	**H20**	**LA15_N**
-	GND	H21	GND
JX2.88	**FMC1_LA19_P**	**H22**	**LA19_P**
JX2.90	**FMC1_LA19_N**	**H23**	**LA19_N**
-	GND	H24	GND
JX2.93	**FMC1_LA21_P**	**H25**	**LA21_P**
JX2.95	**FMC1_LA21_N**	**H26**	**LA21_N**
-	GND	H27	GND
JX2.99	**FMC1_LA24_P**	**H28**	**LA24_P**
JX2.101	**FMC1_LA24_N**	**H29**	**LA24_N**
-	GND	H30	GND
JX2.105	**FMC1_LA28_P**	**H31**	**LA28_P**
JX2.107	**FMC1_LA28_N**	**H32**	**LA28_N**
-	GND	H33	GND
JX1.7	**FMC1_LA30_P**	**H34**	**LA30_P**
JX1.8	**FMC1_LA30_N**	**H35**	**LA30_N**
-	GND	H36	GND
JX1.11	**FMC1_LA32_P**	**H37**	**LA32_P**
JX1.12	**FMC1_LA32_N**	**H38**	**LA32_N**
-	GND	H39	GND
-	FMC_VADJ	H40	VADJ_2.5V

NOTE: The signal pairs highlighted in orange denote pairs that are routed differentially on the Mini-Module Plus Baseboard 2 but may NOT be on the target Mini-Module. Mini-Module specification defines these pins as single ended signals.

2.3 Clock Sources

This section describes the clock sources that are available on the Mini-Module Plus Baseboard 2.

2.3.1 CDCM61001 Programmable Clock Synthesizer

There is an on-board TI CDCM61001 LVDS clock synthesizer that is connected to the MGT_REFCLK inputs on the Mini-Module Plus connector JX1 and can be used to generate the reference clock for the target Mini-Module's GTX circuit(s).

A list of features included in the CDCM61001 device is shown below.

- Output frequency range: 43.75 MHz to 683.264 MHz
- RMS period jitter: 0.509 ps @ 625 MHz
- Output rise and fall time: 255 ps (maximum)
- Output duty cycle: varies dependant on output frequency

The following figure shows a high-level block diagram of the CDCM61001 programmable clock synthesizer. Inputs OS0 and OS1 are hard wired to use the LVDS mode of the CDCM61001 device.

Design Note: The CDCM61001 is sourced by a 27 MHz clock oscillator U10.

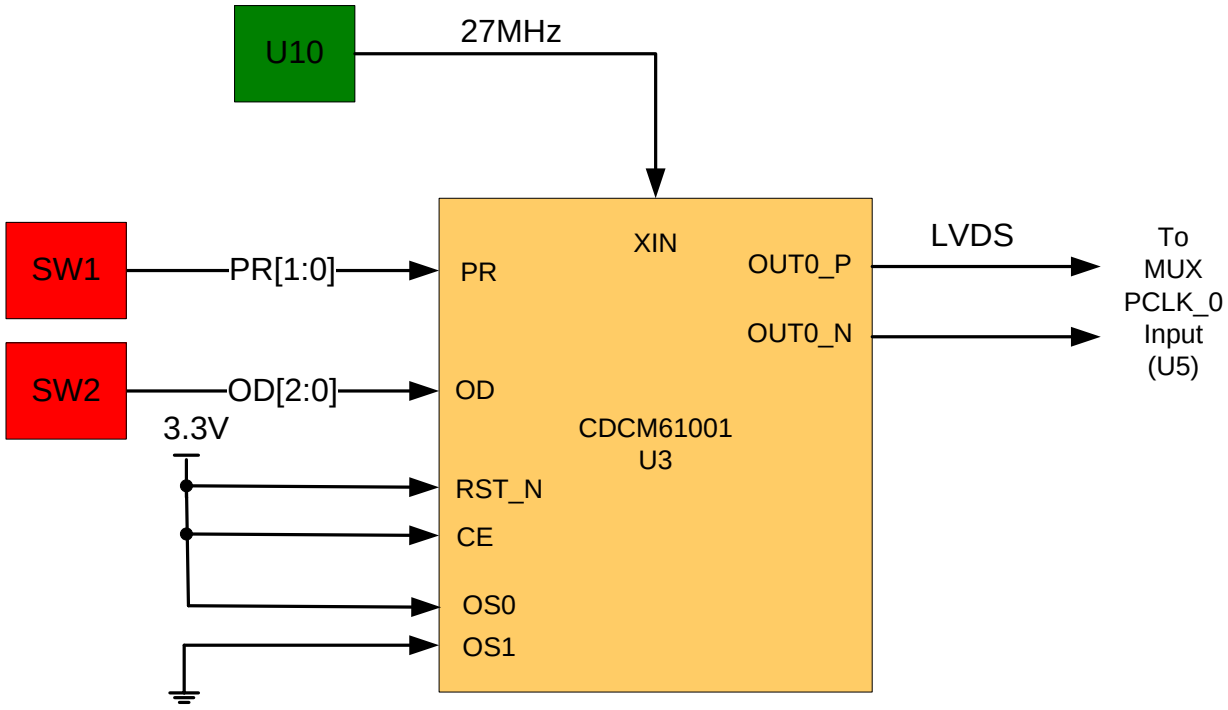


Figure 11 - CDCM61001 Clock Synthesizer

Table 15 - CDCM61001 Clock Synthesizer Pin Description

Signal Name	Direction	Pull up/Pull down (Internal)	Description
PR[1:0]	Input	Pull up	Prescaler and Feedback divider control pins.
OD[2:0]	Input	Pull up	Output divider control pins.
OS[1:0]	Input	Pull up	Output type select control pins.
CE	Input	Pull up	Chip enable.
RST_N	Input	Pull up	Device reset (active low).
XIN	Input	Pull up	Parallel resonant crystal/LVCMOS input.
OUT0 P/N	Output		Differential output pair.

2.3.1.1 CDCM61001 Clock Generation

The CDCM61001 output clocks are generated based on the following formula:

FOUT = (FIN) (FD) / OD

Equation Variables:
FOUT = Output Frequency
FIN = Clock Input Frequency
FD = Feedback Divider Value
OD = Output Divider Value

Please refer to the CDCM61001 datasheet for detailed tables regarding the Feedback Divider and Output Divider values. The CDCM61001 FD and OD values are programmed via dipswitches SW1 and SW2. These dipswitches should be configured prior to powering up the board.

2.3.1.2 CDCM61001 Programming Mode

The Mini-Module Plus Baseboard 2 development board allows programming of the PR and OD values in parallel mode. This is the only mode allowed by the device. In parallel mode, PR and OD values are programmed into the device upon power-on. The switches should be set into the correct position prior to turning on power to the board. Should the switch settings change after power up the board will have to be power cycled to reset the device

2.3.2 CDCE913 Programmable Clock

The CDCE913 is a modular PLL-based low-cost, high-performance, programmable clock synthesizer, multiplier, and divider. It can generate up to 3 output clocks from a single input frequency. Each output can be programmed via an SDA / SCL, SMBus / I2C interface, for any clock frequency up to 230 MHz, using the integrated configurable PLL. The input crystal frequency for the CDCE913 is 27MHz.

Only two of the outputs on the CDCE913 are used on the Mini-Module Plus Baseboard 2. The CDCE913 clock outputs will connect to global clock inputs on the target Mini-Module. The Y3 output is left floating.

The table below shows the electrical connection between the CDCE913 clock generator and the Mini-Module Plus connectors.

Table 16 – CDCE913 Pin Assignments

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
CDCE_SCL	JX1.34
CDCE_SDA	JX1.33
CDCE_Y1_OUT	JX1.39
CDCE_Y2_OUT	JX2.39

2.4 Communication

The Mini-Module Plus Baseboard 2 Implements a Silicon Labs CP2102 device that provides a USB-to-RS232 bridge. The USB physical interface is brought out on a USB Type-B connector labeled “J8”.

The USB-to-RS232 bridge interface connects to the Mini-Module Plus connectors at the following pins:

Table 17 – USB-to-RS232 Pin Assignments

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
UART_TX	JX1.36
UART_RX	JX1.35

2.5 Memory

The Mini-Module Plus Baseboard 2 implements a Micro-SD Card interface. The table below shows how the Micro-SD Card connector connects to the Mini-Module Plus connectors.

Table 18 – Micro-SD Card Pin Assignments

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
SD1_D0	JX2.32
SD1_D1	JX2.33
SD1_D2	JX2.34
SD1_D3	JX2.35
SD1_CMD	JX2.36
SD1_CLK	JX2.37

2.6 PMOD Headers

Two vertical, 12-pin (2 x 6 female) Peripheral Module (PMOD) headers (J2, J5) are connected to the Mini-Module Plus connectors, with each header providing 3.3 V power, ground, and eight I/O's. These headers may be utilized as general-purpose I/Os or may be used to interface to PMODs. J2 and J5 are placed in close proximity (0'9"-centers) on the PCB in order to support dual PMODs. Tables 19 and 20 provide the connector and FPGA pin out. For Digilent PMODs see:

http://www.digilentinc.com/Products/Catalog.cfm?Nav1=Products&Nav2=Peripheral&Cat=Peripheral

Table 19 - Peripheral Module Pin Assignments – J2

Mini-Module Plus mating Connector (JX2)	I/O Signal	Connector Pin #	Connector Pin #	I/O Signal	Mini-Module Plus mating Connector (JX2)
JX2.14	PMOD1_P1	1	2	PMOD1_P2	JX2.15
JX2.16	PMOD1_P3	3	4	PMOD1_P4	JX2.17
-	**GND**	5	6	**3.3V**	-
JX2.18	PMOD1_P7	7	8	PMOD1_P8	JX2.19
JX2.20	PMOD1_P9	9	10	PMOD1_P10	JX2.23
-	**GND**	11	12	**3.3V**	-

Table 20 - Peripheral Module Pin Assignments – J5

Mini-Module Plus mating Connector (JX2)	Signal Name	Connector Pin #	Connector Pin #	Signal Name	Mini-Module Plus mating Connector (JX2)
JX2.24	PMOD2_P1	1	2	PMOD2_P2	JX2.25
JX2.26	PMOD2_P3	3	4	PMOD2_P4	JX2.27
-	**GND**	5	6	**3.3V**	-
JX2.28	PMOD2_P7	7	8	PMOD2_P8	JX2.29
JX2.30	PMOD2_P9	9	10	PMOD2_P10	JX2.31
-	**GND**	11	12	**3.3V**	-

2.7 User Push Buttons and Switches

Four momentary closure push buttons have been installed on the board and connected to the Mini-Module Plus connectors. These buttons can be programmed by the user on the target Mini-Module's FPGA and are ideal for logic reset and similar functions. Pull down resistors hold the signals low until the switch closure pulls them high (active high signals).

Table 21 - Push Button Pin Assignments

Signal Name	Reference	Mini-Module Plus mating Connector (JX2)
PB0	SW7	JX2.3
PB1	SW8	JX2.4
PB2	SW9	JX2.5
PB3	SW10	JX2.6

An eight-position dipswitch (SPST) has been installed on the board and connected to the Mini-Module Plus connectors. These switches provide digital inputs to user logic as needed. The signals are pulled low by 4.7K ohm resistors when the switch is open and tied high to FMC_VADJ (see "Power" section) when closed as shown in the following table.

Table 22 - DIP Switch Pin Assignments

Signal Name	Reference	Voltage when closed	Mini-Module Plus mating Connector (JX1)
SW0	SW6 – 1	FMC_VADJ	JX1.17
SW1	SW6 – 2		JX1.18
SW2	SW6 – 3		JX1.19
SW3	SW6 – 4		JX1.20
SW4	SW6 – 5		JX1.23
SW5	SW6 – 6		JX1.24
SW6	SW6 – 7		JX1.25
SW7	SW6 – 8		JX1.26

2.8 User LEDs

Five discrete LEDs are installed on the board and can be used to display the status of the target Mini-Module FPGA's internal logic. These LEDs are attached as shown below and are lit by forcing the associated FPGA I/O pin to a logic '1' and are off when the pin is either low (0) or not driven.

Table 23 - LED Pin Assignments

Net Name	Reference	Mini-Module Plus mating Connector (JX1)
LED0	D20	JX1.27
LED1	D21	JX1.28
LED2	D22	JX1.29
LED3	D23	JX1.30
LED4	D24	JX1.31

2.9 Configuration

The Mini-Module Plus Baseboard 2 supports two methods of configuring the target Mini-Module's FPGA. Both configuration sources use Boundary-scan and use either the Xilinx platform JTAG cable (J1) or the Digilent HS1 USB-JTAG module (U1). The blue "DONE" LED (D1) on the board illuminates to indicate when the FPGA has been successfully configured.

2.9.1 JTAG Chain

The Mini-Module Plus Baseboard 2 has two connectors in the JTAG chain, the Mini-Module plus mating connectors and the FMC LPC connector. The following figure shows a high-level block diagram of the JTAG Chain on the development board.

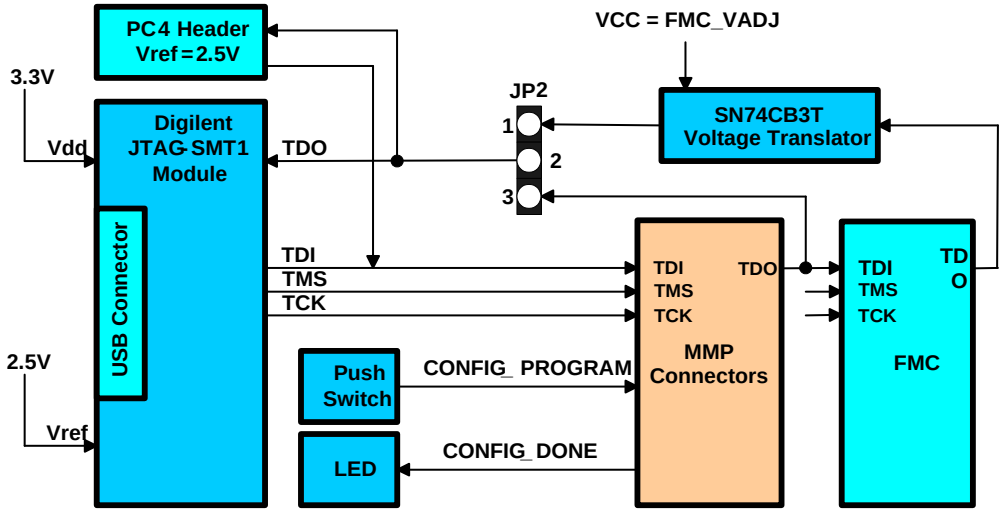


Figure 12 - JTAG Chain on the Mini-Module Plus Baseboard 2

Configuring the JTAG chain to include one or both can be done using jumper JP2. Setting the jumper position to 1-2 will include both connectors, while placing the jumper to position 2-3 includes only the Mini-Module Plus connectors.

Programming the FPGA on the target Mini-Module via Boundary-scan mode requires either JTAG download cable (not included in the kit). The Xilinx PC4 download cable plugs into the J1 connector on the board. Alternately, a standard USB A-Micro-B cable can be used to configure the target FPGA by plugging it into the Micro-B connector located at U1.

2.10 Power

The Mini-Module Plus Baseboard 2 power is derived from a +12 V input provided by the furnished power supply at J4 or from the 4-pin ATX power connector JP1. No power is available to the baseboard through the PCI Express edge connector. All of the voltage rails used on the board are derived from the 12V source. The 12V source is used to supply the input voltages to a variety of power solutions that reside power modules that are available from Avnet for the baseboard. This modular power approach allows the user to pick the best power solution for the end application and also allows the user flexibility to design their own power module if desired.

Avnet currently offers pre-designed power module solutions from Texas Instruments, Maxim, General Electric, ST Micro and Analog Devices. Click on the following link to the Avnet Design resource Center (DRC) to get more details.

http://avnet.com/us/design/drc/Pages/Xilinx-Kintex-7-Mini-Module-Plus.aspx

The voltage rails produced by the power modules are: 1.5V/1.35V (jumper selectable on the power modules), 1.8V, 2.0V, 3.3V, 1.0V, 1.0V_MGT, and 1.2V_MGT.

In stand-alone mode the board is connected to the external power supply via the six pin right angle connector J4**.** The power supply shipped with the Mini-Module Plus Baseboard 2 can supply 12 V @ 5 Amps.

NOTICE!!! NOTICE!!! NOTICE!!!

THE 6-PIN CONNECTOR "J4" SHOULD NEVER BE PLUGGED INTO A PC'S ATX 6-PIN PCI EXPRESS POWER CONNECTOR!

THE TWO CONNECTORS ARE NOT COMPATIBLE AND WILL CAUSE DAMAGE TO THE PC POWER SUPPLY, MINI-MODULE PLUS BASEBOARD 2, MINI-MODULE, POWER MODULE OR ALL OF THE ABOVE!

THE CONNECTOR "J4" WILL HAVE THE FOLLOWING LABEL ADHERED TO ITS TOP SIDE:

When the Mini-Module Plus Baseboard 2 is plugged into a PCI Express slot within the PC's chassis it is recommended that the 4-pin ATX power connector JP1 is used to supply 12V to the board.

The main power switch to for the development board is SW5 and must be turned ON to supply any power to the board.

The figure below shows a high-level block diagram of the power architecture on the development board.

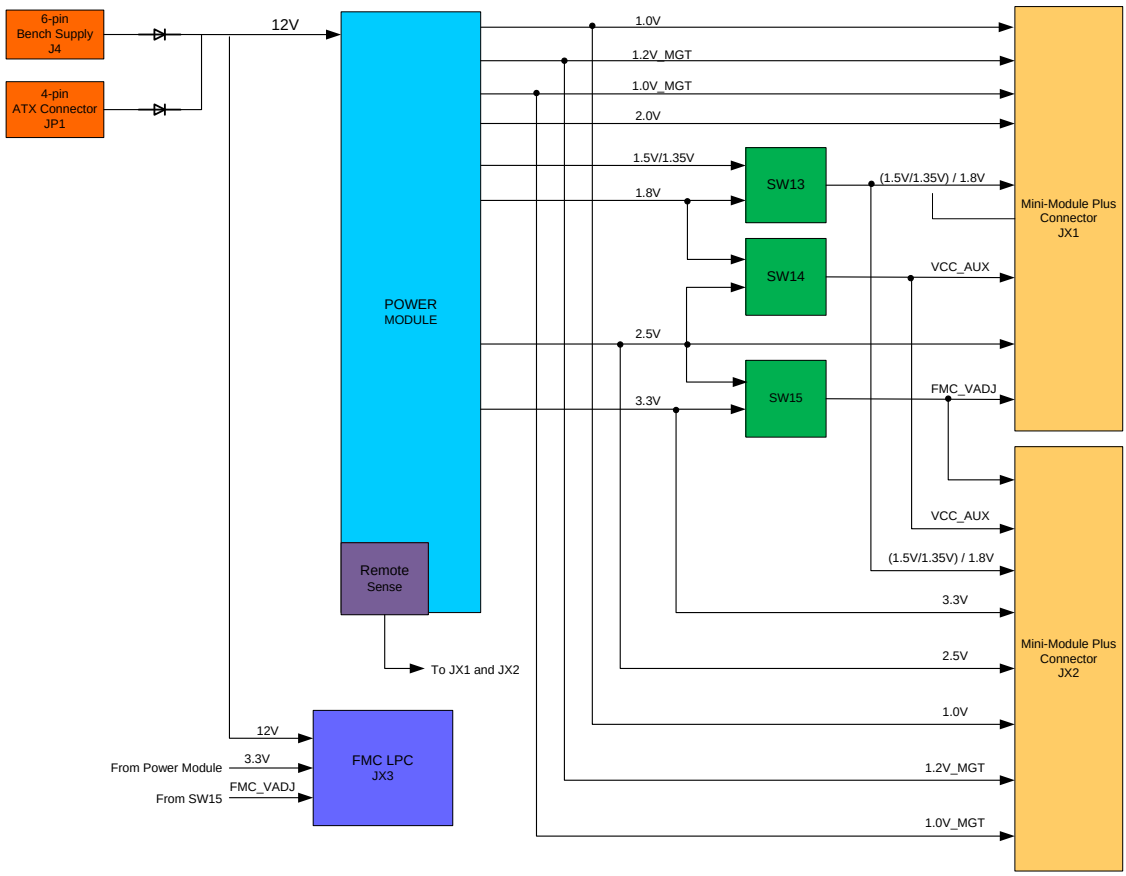


Figure 13 - Board Power

SW13 controls the voltage for the DDR circuits on a given target Mini-Module. Mini-Modules that implement DDR2 memory will utilize the 1.8V rail. Mini-Modules implementing DDR3 memory will use the 1.35/1.5V rail. Since DDR3 core voltage can be either 1.35V or 1.5V, the power modules have a jumper that can be placed to switch between 1.35V and 1.5V. Placing SW13 in the DOWN position selects 1.8V, while placing the switch in the UP position selects 1.35V/1.5V.

NOTE: SW13 is not installed on Rev C boards. The SW13 setting has been hardwired to support K7 Mini-Modules. See the bottom part of this section for details on the hardwired settings and how to modify the setting to support Virtex-5 Mini-Modules.

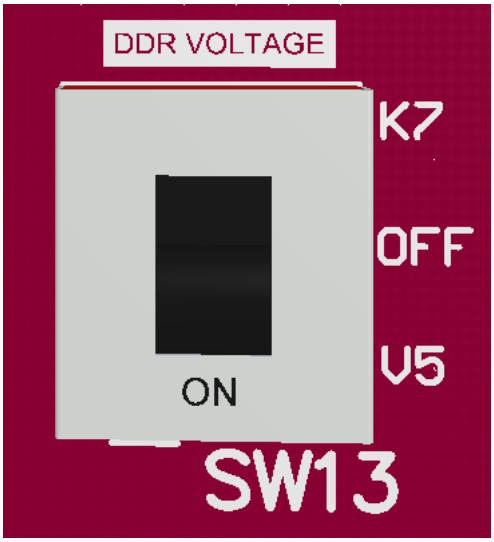


Figure 14 – DDR Voltage SW13

SW14 controls the VCC_AUX voltage being supplied to the target Mini-Module's FPGA. The Mini-Module Plus Baseboard 2 is backward compatible with the Virtex-5 Mini-Module, and thus the reason for this switch. Setting SW14 in the DOWN position sets VCC_AUX = 2.5V for Virtex-5 Mini-Modules. Setting the switch in the UP position sets the VCC_AUX = 1.8V, supporting the Kintex-7 mini-Module.

WARNING! WARNING! WARNING!

SW14 MUST BE SET PROPERLY WHEN INSTALLING A KINTEX-7 MINI-MODULE!! THE SWITCH MUST BE SET IN THE "UP" POSITION TO PREVENT DAMAGE TO THE KINTEX-7 FPGA. INSURE THE PROPER SWITCH SETTING PRIOR TO APPLYING POWER TO THE BOARD!!!

SEVERE DAMAGE TO THE MINI-MODULE CAN OCCUR IF THIS SWITCH IS NOT SET PROPERLY!!!

WARNING! WARNING! WARNING!

NOTE: SW14 is not installed on Rev C boards. The SW14 setting has been hardwired to support K7 Mini-Modules. See the bottom part of this section for details on the hardwired settings and how to modify the setting to support Virtex-5 Mini-Modules.

Figure 15 – VCC_AUX Voltage SW14

SW15 controls the FMC_VADJ voltage. The setting is either 2.5V or 3.3V. This setting is completely application specific. If an FMC module is installed on the baseboard that utilizes 3.3V I/O then setting this switch to the 3.3V position insures that the I/O routed to the FPGA banks connected to the FMC module will operate at the correct I/O voltage for the application.

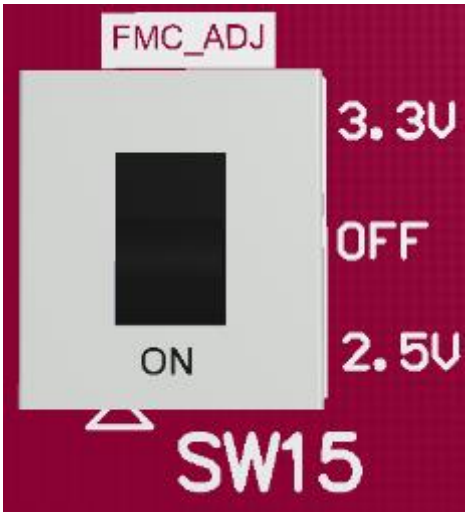


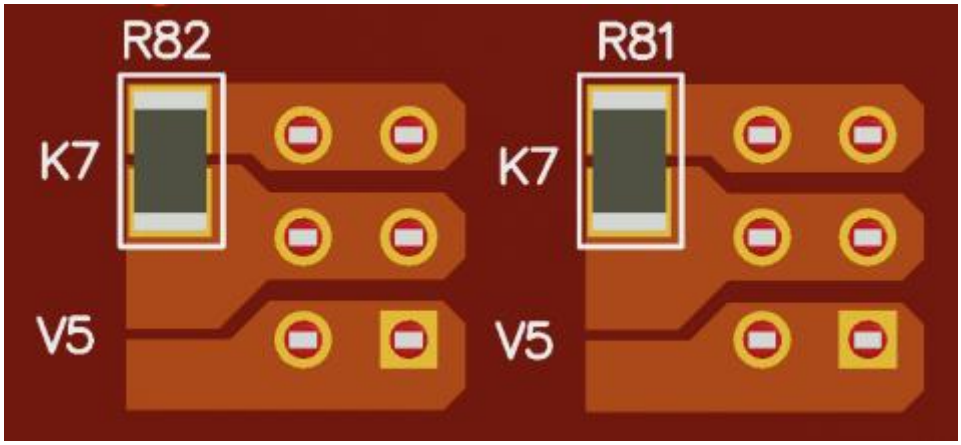
Figure 16 – FMC VADJ Voltage SW15

SW13 and SW14 Rev C Hardwired Settings

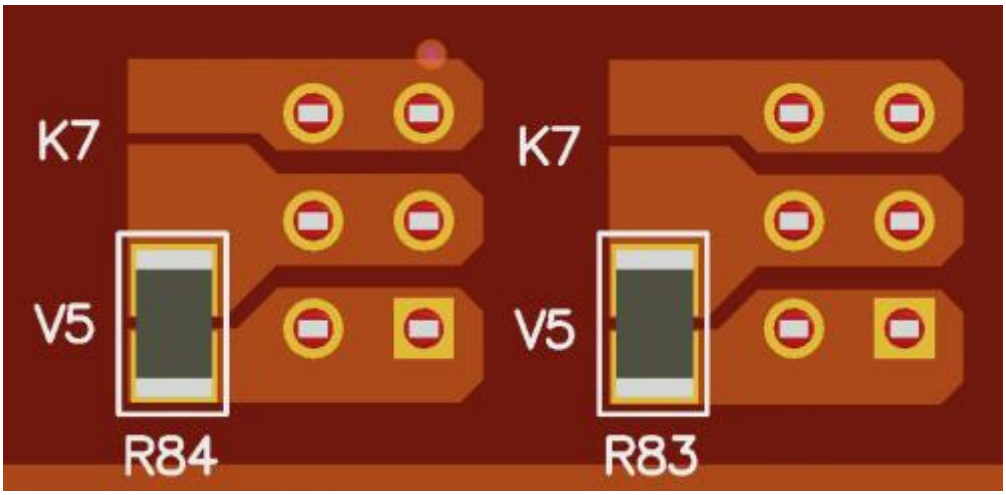
As mentioned in the above notes, SW13 and SW14 have been removed on Rev C Mini-Module Plus Baseboard's 2. The switches have jumper pads on the bottom side of the board directly below the switches that allow the user to hardwire the appropriate voltages for the DDR3 and VCC_AUX voltage rails depending on which platform is being used; Kintex-7 or Virtex-5. The jumpers used for Rev C boards are 0-ohm resistors in a 2512 package. The change on the Rev C boards came as a result of users inadvertently causing damage to the Kintex-7 Mini-Modules and/or DDR3 memory by having the switches set or inadvertently moved to the wrong position.

The default circuits for SW13 and SW14 is set to support the Kintex-7 platform which supplies 1.8V to VCC_AUX (SW14) and 1.5 or 1.35V to the DDR3 memory (SW13). The DDR memory voltage is determined by a jumper on the power modules.

See the picture below for an illustration of the default (K7) jumper positions as shipped from the factory.



If the user intends to support the Virtex-5 Mini-Module Plus platform, the jumpers must be moved to change the voltage settings for VCC_AUX (2.5V) and DDR2 memory (1.8V). The illustration below shows the proper implementation of the jumpers to support the Virtex-5 platform.



2.10.1 Remote Sense

The Mini-Module Plus Baseboard 2 implements remote sense in its power architecture using two connectors. One is located near the power module and plugs directly into the power module and is designated by J7. The other is located near the Mini-Module plus connectors and is designated J10.

Remote sense is implemented to insure more accurate voltage regulation at the loads of the target Mini-Module. The Kintex-7 Mini-Module from Avnet implements the remote sense connector. The Virtex-5 Mini-Module does not support the remote sense feature.

For Mini-Modules that implement remote sense feedback, the remote sense signals are placed at strategic and/or critical places at the various Mini-Module loads. Those signals are then routed down to the J10 connector on the baseboard and fed back to the power module for precise load regulation on a per rail basis.

Remote sense can be disabled by the user by moving or removing the 0-ohm jumper resistors on the baseboard. The default position of the resistor jumpers is in position 1-2, which enables the remote sense feedback path to the power module regulators. Moving the resistor jumpers to the 2-3 position ties the remote sense feedback loop directly to the regulated output voltage per rail. This may or may not be desirable depending on the implementation of power module's remote sense feedback loop.

It is recommended that the remote sense feature be left enabled. For Mini-Modules that implement the remote sense feedback the voltages on each rail will be much more stable and efficient. For Mini-Modules that do not use the remote sense feedback the circuits on the power module will remain unaffected.

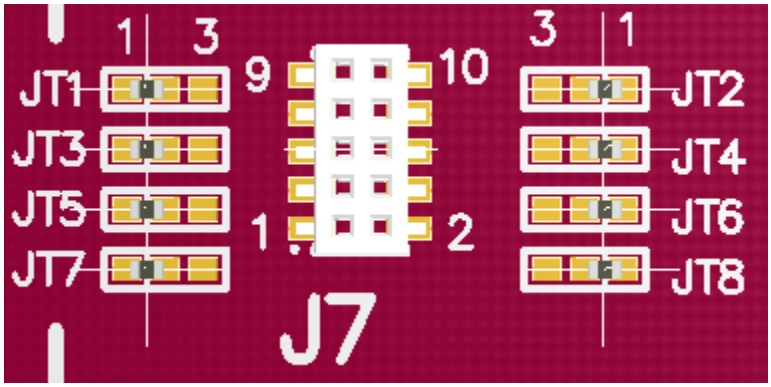


Figure 17 – Remote Sense Configuration Resistors

2.11 Thermal Management

The Mini-Module Plus Baseboard 2 provides a 12V connector that can be used to plug in a 12V active heat sink/fan assembly. The Virtex-5 Mini-Module does not come shipped with the active heat sink, but the K7 Mini-Module Plus and possible future Mini-Module designs could use one. Virtex-5 Mini-Module customers that use the Mini-Module Plus Baseboard 2 that wish to use an active heat sink can do so by using the information provided below. The 12V connector provided is implemented differently on Revision B baseboards than it is on revision C baseboards.

2.11.1 Revision B Baseboards

Revision B baseboards were not originally designed to implement the 12V fan connector. Revision B baseboards have been reworked to add the wires and the connector. See the below picture to see how the 12V fan connector is wired and attached to the baseboard.

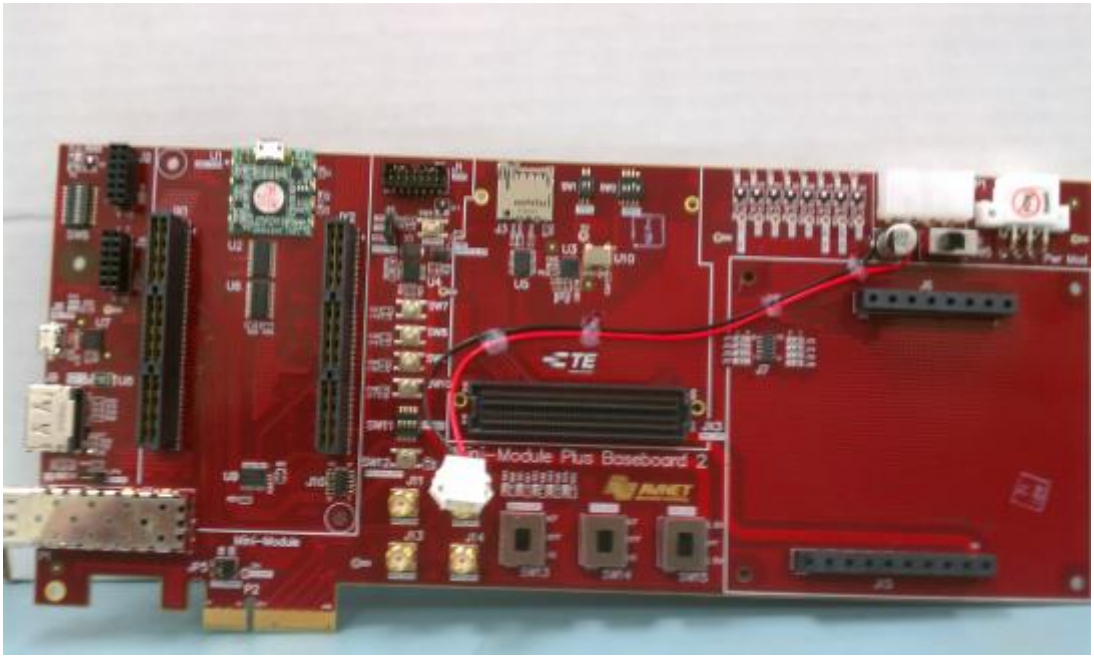


Figure 18 – 12V Fan Connector, Revision B Baseboards

The parts used to make this board modification follow:

- (1)6.5", Red, 26 gauge wire
- (1)6.5", Black, 26 gauge wire
- (1)TE 173977-3
- (1)TE 292254-3 (alternate = 292156-3)

The red wire is soldered to the positive terminal of C7 and the black wire is soldered to the negative terminal of C7.

2.11.2 Revision C Baseboards

Revision C baseboards will have the 12V fan connector soldered onto the board and the 12V connected to it internal to the board stack-up. The part number used for the fan connector on Revision C baseboards is TE 292161-3.

This two-position header can be identified on the board as J16.

3 Test and Reference Designs

Test and reference designs for the currently available Avnet Mini-Modules are provided at the Design Resource Center (DRC) web site under the "Support and Download Files" section:

Kintex-7 Mini-Module
http://avnet.com/us/design/drc/Pages/Xilinx-Kintex-7-Mini-Module-Plus.aspx

Virtex-5 FXT Mini-Module
http://avnet.com/us/design/drc/Pages/Xilinx-Virtex-5-FXT-Mini-Module-Plus.aspx

4 References

- Virtex-5 Mini-Module Plus User's Guide
- Kintex-7 Mini-Module plus User's Guide

5 Appendix A

This section provides a description of the jumper settings and switches for the Mini-Module Plus Baseboard 2. The board is ready to use out of the box with the default jumper settings.

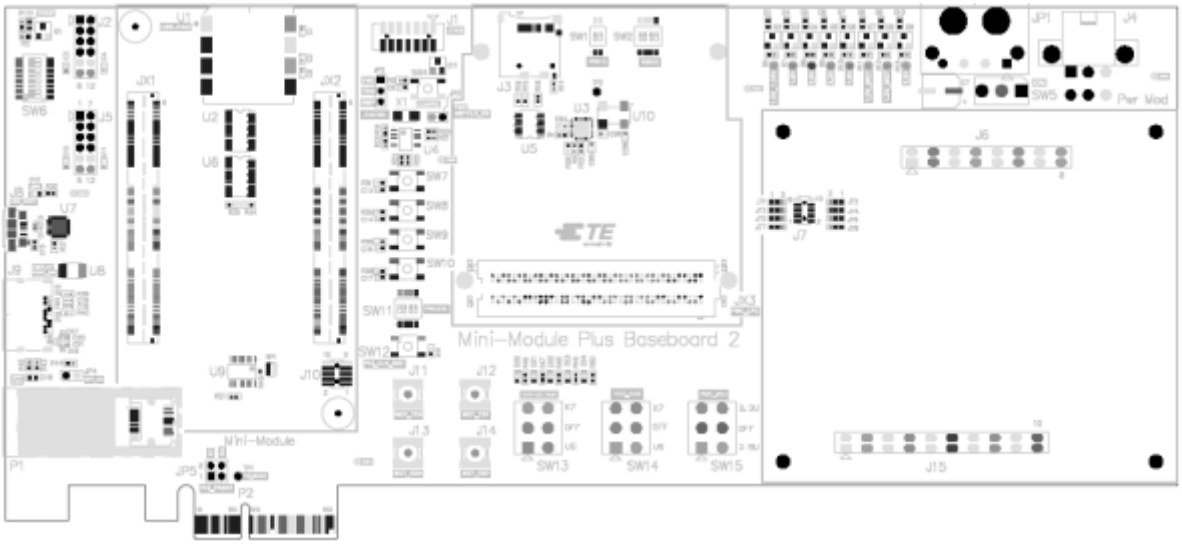


Figure 19 - Board Assembly Drawing

JP2 "JTAG SEL" – Configures the JTAG chain to either include just the target Mini-Module or to include the FMC LPC slot as well. Position 1:2 includes both the Mini-Module Plus and the FMC slot. Position 2:3 includes only the Mini-Module Plus. Default: JP2 2:3 (Mini-Module Plus only).

JP3 "FMC GBTCLK_EN" – Enables the FMC GBTCLK signal to pass through the 2:1 differential MUX (U5). With no jumper shunt placed the output of the CDCM61001 programmable clock synthesizer (U3) is passed to the Mini-Module Plus connectors as the JX1 MGT reference clock. Default: Open (CDCM61001 output).

JP4 – SFP Enable, install a shunt to enable a module plugged into the Small Form Pluggable (SFP) cage labeled "P1" on the board. Default: Closed (enabled).

JP5 "PCI_PRSNT" – Selects the number of PCI Express lanes to advertise to the host PC. A single jumper is installed to connect the PRSNT1# pin to the PRSNT2# pin that corresponds to the desired lane width (x1 or x4). This allows the user to force fewer lanes to be used to target applications requiring less than 4 lanes. Default: JP1 3:4 (4 lanes).

J2 "SFP EN" – SFP Enable, install a shunt to enable a module plugged into the Small Form Pluggable (SFP) cage labeled "P2" on the board. Default: Closed (enabled).

SW1 and SW2 "PR[1:0] and OD[2:0]" – These switches control the output frequency of the CDM61001 LVDS clock synthesizer. Refer to section 2.1.1 for more details.

SW4 "CONFIG" – Depressing and releasing this switch will force the target FPGA to reconfigure itself. Reconfiguration does not occur if the FPGA is in the JTAG configuration mode.

SW5 – This switch is the main power switch to the board. Regardless of what 12V source is being used to power the board this switch must be ion the ON position to power the board.

SW6 – This eight position dip-switch can be used as GPIO inputs to the target FPGA. The switch(s) logic level is default LOW until the switch is toggled. When toggled ON, the logic level to the IO pin is HIGH (3.3 V).

SW7, SW8, SW9, and SW10 – These push button switches can be used as GPIO inputs to the target FPGA. The switch(s) logic level is default LOW until the switch is pushed. When pushed ON, the logic level to the IO pin is HIGH (FMC_VADJ).

SW11 "FS 2-1-0" – This 4-position switch is used to configure the output frequency of the ICS874003-05 jitter attenuator. Refer to Section 2.2.2 for more details.

SW12 – This switch is a master reset switch for the ICS874003-05 jitter attenuator device. Depressing and releasing this switch will reset U9.

SW13 "DDR VOLTAGE"- Controls the DDR core voltage forwarded to the Mini-Module Plus. If the switch is DOWN (V5) 1.8V will be sourced to the Mini-Module for DDR2 memory circuits. If the switch is in the IUP (K7) position either 1.35V or 1.5V will be sourced to the Mini-Module. The 1.35V vs. 1.5V is determined by a jumper on the power module. Default: UP (DDR Voltage = 1.35V/1.5V)

SW14 "VCC AUX" – Controls the VVC AUX voltage forwarded to the Mini-Modules target FPGA. If the switch is in the DOWN (V5) position 2.5V will be sourced. If the switch is in the UP position (K7) then 1.8V will be sourced. Default: UP (VCC_AUX = 1.8V)

IMPORTANT!!!! Make sure this switch is set properly prior to turning on power to the board with a Mini-Module attached!!! Damage may occur to the target FPGA if this switch is not set properly!!!

SW15 "FMC_VADJ" – Controls the voltage being supplied to the FMC LPC slots VADJ pins and the Mini-Module Plus target FPGA bank IO voltage (VCCO). Depending on the FMC module application, this may be set to 2.5V or 3.3V. Default: DOWN (2.5V).