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1 INTRODUCTION
This document provides information for designing a custom system carrier card for PicoZed. It includes reference schematics for the external circuitry required to implement the various PicoZed peripheral functions. It also explains how to extend the supported busses and how to add additional peripherals and expansion slots.

1.1 Glossary

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIO</td>
<td>Multiplexed Input Output – the dedicated I/O available on the PS</td>
</tr>
<tr>
<td>PL</td>
<td>Programmable Logic</td>
</tr>
<tr>
<td>POR</td>
<td>Power On Reset</td>
</tr>
<tr>
<td>PS</td>
<td>Processing System</td>
</tr>
</tbody>
</table>

1.2 Additional Documentation
Additional information and documentation on Xilinx’s Zynq®-7000 All Programmable SoCs can be found at [www.xilinx.com/zynq](http://www.xilinx.com/zynq). Additional information and documentation on PicoZed can be found at [www.picozed.org](http://www.picozed.org).
2 PICOZED OPTIONS
PicoZed comes in 7010, 7015, 7020, and 7030 versions. Additionally, each version is offered populated with Commercial temperature grade (0° C to 70° C) or Industrial temperature Grade (-40° C to 85° C).

2.1 PL Resources
The resource comparison between the various Zynq devices can be seen in Xilinx document XMP087.

2.2 PL I/O
PicoZed connects 50 I/Os from both Bank 34 and Bank 35. Additionally, the PicoZed 7020 version adds another 25 I/O from Bank 13 while the PicoZed 7015 and 7030 add a total of 35 I/O from Bank 13. The MicroHeaders provide for independent Vccio pins for Bank 13, which provides for additional voltage flexibility. Please note the PL IO Bank power rails (Vccio_34, Vccio_35, and Vccio_13 [7015/7020/7030 versions]) must be powered from a Carrier Card via JX1, JX2, and JX3 if used.

2.3 Transceiver I/O
The 7010 and 7020 devices do not support transceivers and thus PicoZed with the 7010 or 7020 does not populate the JX3 MicroHeader with the transceiver signals or transceiver power. In this case, you can omit the requirement of providing connections to the transceiver signals or providing transceiver power rails from the Carrier Card design.

The PicoZed 7015/7030 offers GTP transceivers in the 7015 and GTX transceivers in the 7030. The Carrier Card design should carefully examine desired performance requirements of the transceivers and provide adequate signaling and transceiver power on the associated pins of the JX3 connector. In the case where the transceivers are not needed, the Carrier Card should take care to follow the UNUSED TRANSCEIVER guidelines defined in the respective Transceiver User Guide.

NOTE: The transceivers differ between the 7015 and the 7030 in power requirements and care should be taken depending on which platform is desired in your system. Review the Transceiver User's Guides for details surrounding the difference between designs using the 7015 versus the 7030.

2.4 Thermal
The wide range of devices supported by PicoZed has significantly varying internal PL resources. Take care to design a thermal management system to account for your final design needs. PicoZed has provided a 3.3V/5V Active Fan header and the 7010/7020 modules provide thru-holes for push-pin heat sinks.
3 PICOZED INTERFACES
A Carrier Card may utilize several Zynq interfaces on the PicoZed. A table showing the Signals, Pin Count, and Zynq source is shown below.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Source</th>
<th>Pin Count</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PL</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank 34 I/Os (except for PUDC_B)</td>
<td>Zynq Bank 34 or Zynq Bank 35</td>
<td>49 **</td>
</tr>
<tr>
<td>Bank 13 I/Os</td>
<td>Zynq Bank 13</td>
<td>8 **</td>
</tr>
<tr>
<td><strong>JTAG</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMS_0</td>
<td>Zynq Bank 0</td>
<td></td>
</tr>
<tr>
<td>TDI_0</td>
<td>Zynq Bank 0</td>
<td></td>
</tr>
<tr>
<td>TCK_0</td>
<td>Zynq Bank 0</td>
<td></td>
</tr>
<tr>
<td>TDO_0</td>
<td>Zynq Bank 0</td>
<td></td>
</tr>
<tr>
<td>Carrier_SRST#</td>
<td>Carrier</td>
<td></td>
</tr>
<tr>
<td><strong>Analog</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VP_0</td>
<td>Zynq Bank 0</td>
<td></td>
</tr>
<tr>
<td>VN_0</td>
<td>Zynq Bank 0</td>
<td></td>
</tr>
<tr>
<td>DXP_0</td>
<td>Zynq Bank 0</td>
<td></td>
</tr>
<tr>
<td>DXN_0</td>
<td>Zynq Bank 0</td>
<td></td>
</tr>
<tr>
<td><strong>C</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PUDC_B / IO</td>
<td>Zynq Bank 34</td>
<td>2</td>
</tr>
<tr>
<td>DONE</td>
<td>Zynq Bank 0</td>
<td></td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWR_Enable</td>
<td>Carrier</td>
<td>1</td>
</tr>
<tr>
<td>Vin</td>
<td>Carrier</td>
<td>4</td>
</tr>
<tr>
<td>GND</td>
<td>Carrier</td>
<td>23</td>
</tr>
<tr>
<td>VCCO_34</td>
<td>Carrier</td>
<td>3</td>
</tr>
<tr>
<td>VBATT</td>
<td>Carrier</td>
<td>1</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td>100</td>
</tr>
</tbody>
</table>

Table 1 – JX1 MicroHeader Pinout

** PicoZed 7015/7020/7030
## PicoZed 7010/7020 Bank 34 and PicoZed 7015/7030 Bank 35
### MicroHeader #2 (JX2)

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Source</th>
<th>Pin Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>PL Bank 35 I/Os</td>
<td>Zynq Bank 35 or Zynq Bank 34</td>
<td>50 **</td>
</tr>
<tr>
<td>Bank 13 I/Os</td>
<td>Zynq Bank 13</td>
<td>7 **</td>
</tr>
<tr>
<td>PS PS MIO [0,9-15]</td>
<td>Zynq Bank 500</td>
<td>8</td>
</tr>
<tr>
<td>C Init_B_0</td>
<td>Zynq Bank 0</td>
<td>1</td>
</tr>
<tr>
<td>Power VCCIO_EN</td>
<td>Module/Carrier</td>
<td>1</td>
</tr>
<tr>
<td>Power PG_MODULE</td>
<td>Module/Carrier</td>
<td>1</td>
</tr>
<tr>
<td>Power Vin</td>
<td>Carrier</td>
<td>5</td>
</tr>
<tr>
<td>Power GND</td>
<td>Carrier</td>
<td>23</td>
</tr>
<tr>
<td>Power VCCO_13</td>
<td>Carrier</td>
<td>1</td>
</tr>
<tr>
<td>Power VCCO_35</td>
<td>Carrier</td>
<td>3</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td>100</td>
</tr>
</tbody>
</table>

Table 2 – JX2 MicroHeader Pinout

** PicoZed 7015/7020/7030
## PicoZed 7010/7020 Bank 35 and PicoZed 7015/7030 Bank 34

### MicroHeader #3 (JX3)

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Source</th>
<th>Pin Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>PL Bank 13 I/Os</td>
<td>Zynq Bank 13</td>
<td>20 **</td>
</tr>
<tr>
<td>XCVR MGTTX I/Os</td>
<td>Zynq Bank 112</td>
<td>20 **</td>
</tr>
<tr>
<td></td>
<td>MGTTRX I/Os</td>
<td>20 **</td>
</tr>
<tr>
<td></td>
<td>MGTREFCLK I/Os</td>
<td>20 **</td>
</tr>
<tr>
<td>PS MIQ[40-51]</td>
<td>Zynq Bank 501</td>
<td>26</td>
</tr>
<tr>
<td>Power USB 2.0</td>
<td>Zynq Bank 500</td>
<td></td>
</tr>
<tr>
<td>Power USB_VBUS_OTG</td>
<td>Carrier</td>
<td>1</td>
</tr>
<tr>
<td>Power VCCO_13</td>
<td>Carrier</td>
<td>2</td>
</tr>
<tr>
<td>Power MGTAVCC</td>
<td>Carrier</td>
<td>4</td>
</tr>
<tr>
<td>Power MGTAVTT</td>
<td>Carrier</td>
<td>2</td>
</tr>
<tr>
<td>Power GND</td>
<td>Carrier</td>
<td>25</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td>100</td>
</tr>
</tbody>
</table>

Table 3 – JX3 MicroHeader Pinout

** PicoZed 7020 has 10 I/O and PicoZed 7015/7030 adds 20 I/O
## PicoZed 7015/7030 only
3.1 PS

3.1.1 MIO BANK 500

Eight PS MIOs (0, 9-15) are shared between the eMMC on-board PicoZed and the JX2 MicroHeader. Care must be taken when it is desired to use the eMMC and the PS MIO signals that go to the carrier card.

A multiplexer has been implemented on PicoZed to allow these interfaces to be shared depending on the customers end design. The multiplexer select line is capable of being controlled via MIO0 from a SW perspective or the select line can be fixed via a hardware pull-up or pull-down resistor on PicoZed. By default, the multiplexer select line is pulled down selecting the eMMC interface on PicoZed. In the scenario where MIO0 is used to control the select line via software, MIO0 is unavailable on the JX2 PS interface and the end user should not utilize the MIO0 pin from the carrier card. This leaves the JX2 PS interface at 7 processor pins.

If it is desired that the user only utilize the JX2 PS interface, the proper solution would be to set the PS_MIO0_SEL resistor to select the JX2 PS interface. The PS_MIO0_SEL resistor can be set to select the JX2 PS interface, and the PS_MIO0 resistor can be set to PS_MIO0_MUX in order to make MIO0 available on the JX2 PS interface. The end user can than utilize the MIO0 pin from the carrier card. This would give the JX2 PS interface all 8 processor pins.

Please review the PicoZed Hardware User Guide for further details surrounding the eMMC / JX2 PS MIO Interface Multiplexer.

<table>
<thead>
<tr>
<th>PicoZed 7015/7030 Pin #</th>
<th>PicoZed 7010/7020 Pin #</th>
<th>MIO</th>
<th>Net Name</th>
<th>JX2 Pin #</th>
<th>JX2 Pin #</th>
<th>Net Name</th>
<th>MIO</th>
<th>PicoZed 7010/7020 Pin #</th>
<th>PicoZed 7015/7030 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 – G16</td>
<td>500 - E9</td>
<td>10</td>
<td>MIO10</td>
<td>1</td>
<td>2</td>
<td>MIO13</td>
<td>13</td>
<td>500 - E9</td>
<td>500 – A17</td>
</tr>
<tr>
<td>500 – B17</td>
<td>500 - C5</td>
<td>14</td>
<td>MIO14</td>
<td>3</td>
<td>4</td>
<td>MIO15</td>
<td>15</td>
<td>500 - C5</td>
<td>500 – E17</td>
</tr>
<tr>
<td>500 – C18</td>
<td>500 - D9</td>
<td>12</td>
<td>MIO12</td>
<td>5</td>
<td>6</td>
<td>MIO11</td>
<td>11</td>
<td>500 - D9</td>
<td>500 – B19</td>
</tr>
<tr>
<td>500 – G17</td>
<td>500 - E6</td>
<td>0</td>
<td>MIO0</td>
<td>7</td>
<td>8</td>
<td>MIO9</td>
<td>9</td>
<td>500 - E6</td>
<td>500 – C19</td>
</tr>
</tbody>
</table>

Table 4 – JX2 PS MIO Connections

3.1.2 MIO BANK 501

Twelve PS MIOs (40-51) are mapped to the JX3 MicroHeader.

<table>
<thead>
<tr>
<th>PicoZed 7015/7030 Pin #</th>
<th>PicoZed 7010/7020 Pin #</th>
<th>MIO</th>
<th>Net Name</th>
<th>JX3 Pin #</th>
<th>JX3 Pin #</th>
<th>Net Name</th>
<th>MIO</th>
<th>PicoZed 7010/7020 Pin #</th>
<th>PicoZed 7015/7030 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>501 – C15</td>
<td>501 - C17</td>
<td>41</td>
<td>PS_MIO41</td>
<td>34</td>
<td>40</td>
<td>PS_MIO47</td>
<td>47</td>
<td>501 - B14</td>
<td>501 - B13</td>
</tr>
<tr>
<td>501 – B12</td>
<td>501 - A9</td>
<td>43</td>
<td>PS_MIO43</td>
<td>36</td>
<td>44</td>
<td>PS_MIO49</td>
<td>49</td>
<td>501 - C12</td>
<td>501 – C9</td>
</tr>
<tr>
<td>501 – B14</td>
<td>501 - B15</td>
<td>45</td>
<td>PS_MIO45</td>
<td>38</td>
<td>64</td>
<td>PS_MIO51</td>
<td>51</td>
<td>501 - B9</td>
<td>501 – C13</td>
</tr>
</tbody>
</table>

Table 5 – JX3 PS MIO Connections
Depending on the desired design solution, multiple Zynq PS peripherals can map to the eight BANK 500 PS MIO pins and the twelve BANK 501 PS MIO pins. A new hardware platform should be designed to enable the desired peripheral. Please review the Zynq SOC TRM, UG585, for the mapping requirements of the various available Zynq PS peripherals when designing a PicoZed carrier card.

### 3.1.3 PS GbE Ethernet and PS USB – Special Considerations

Due to critical timing that exists between the physical PHYs for the Gigabit Ethernet and USB2.0 interfaces to the associated PS controllers in the Xilinx Zynq devices, Avnet has decided to implement the Gigabit Ethernet and USB 2.0 PHYs on the PicoZed SOMs. The outputs of the PHYs are connected to the JX3 MicroHeader. It is the responsibility of the Customer Carrier Card designer to implement the proper connections to an RJ45 connector for Gigabit Ethernet and a USB connector for its USB2.0 interface. The following table depicts the necessary JX3 connections and the two subsequent figures shows examples of the Gigabit Ethernet and USB2.0 implementations that could exist on a PicoZed Carrier Card. It is recommended that these designs be used as an example and that the final solution will be tailored to the solution as required by the specific custom Carrier Card requirements.

<table>
<thead>
<tr>
<th>Net Name</th>
<th>JX3 Pin #</th>
<th>JX3 Pin #</th>
<th>Net Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>ETH_PHY_LED0</td>
<td>47</td>
<td>48</td>
<td>ETH_PHY_LED1</td>
</tr>
<tr>
<td>ETH_MD1_P</td>
<td>51</td>
<td>52</td>
<td>ETH_MD2_P</td>
</tr>
<tr>
<td>ETH_MD1_N</td>
<td>53</td>
<td>54</td>
<td>ETH_MD2_N</td>
</tr>
<tr>
<td>ETH_MD3_P</td>
<td>57</td>
<td>58</td>
<td>ETH_MD4_P</td>
</tr>
<tr>
<td>ETH_MD3_N</td>
<td>59</td>
<td>60</td>
<td>ETH_MD4_N</td>
</tr>
<tr>
<td>USB_OTG_ID</td>
<td>63</td>
<td>68</td>
<td>USB_VBUS_OTG</td>
</tr>
<tr>
<td>USB_OTG_P</td>
<td>67</td>
<td>70</td>
<td>USB_OTG_CPEN</td>
</tr>
<tr>
<td>USB_OTG_N</td>
<td>69</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 6 – JX3 Gigabit Ethernet and USB2.0 Connections**

![Figure 1 – PicoZed Carrier Card Example Gigabit Ethernet Implementation](image-url)
3.1.4 Control

PicoZed routes two system control signals to the MicroHeaders.

<table>
<thead>
<tr>
<th>Function</th>
<th>Signal Name</th>
<th>MicroHeader Connection</th>
<th>Subsection</th>
<th>PicoZed 7010/7020 Pin #</th>
<th>PicoZed 7015/7030 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>External System Reset</td>
<td>CARRIER_SRST#</td>
<td>JX1.6</td>
<td>PS (MIO Bank 501)</td>
<td>B10</td>
<td>C14</td>
</tr>
<tr>
<td>External Power-on-Reset</td>
<td>PG_MODULE</td>
<td>JX2.11</td>
<td>PS (MIO Bank 500)</td>
<td>C7</td>
<td>B18</td>
</tr>
</tbody>
</table>

Table 7 – System Control Signals

External system reset, labeled CARRIER_SRST#, resets the processor as well as erases all debug configurations. The external system reset allows the user to reset all of the functional logic within the device without disturbing the debug environment. For example, the previous break points set by the user remain valid after system reset. Due to security concerns, system reset erases all memory content within the PS, including the OCM. The PL is also reset in system reset. System reset does not re-sample the boot mode strapping pins.

CARRIER_SRST# is an active-low signal. Asserting this signal asserts Zynq signal PS_SRST_B.

If this pin is not used in the system, it can be left floating since it is pulled up on the PicoZed.
**Note:** This signal cannot be asserted while the boot ROM is executing following a POR reset. If PS_SRST# is asserted while the boot ROM is running through a POR reset sequence it will trigger a lock-down event preventing the boot ROM from completing. To recover from lockdown the device either needs to be power cycled or PS_POR_B needs to be asserted.

The Zynq PS supports an external power-on reset signal. The power-on reset is the master reset of the entire chip. This signal resets every register in the device capable of being reset. This signal, labeled PG_MODULE, is connected to the power good output of the final stage of the power regulation circuitry. These power supplies have open drain outputs that pull this signal low until the output voltage is valid. A carrier card should also wire-OR to this net and not release it until the carrier card power is also good. Other IC's on PicoZed are reset by this signal as well.

The signal can also be actively pulled low to initiate a power-on reset.

To stall Zynq boot-up, this signal should be held low. Other typical FPGA architecture signals (SRST, PROGRAM_B, INIT_B) are not capable of performing this function.

### 3.2 PL IO SIGNALS

PicoZed connects 50 I/Os from both Bank 34 and Bank 35. Additionally, the PicoZed 7020 version adds another 25 I/O from Bank 13 while the PicoZed 7015 and 7030 add a total of 35 I/O from Bank 13. Each of these banks has independent power pins for Vcco on the MicroHeaders. When flexibility in voltage standard is needed, each bank can be powered from a separate regulator. When cost is a concern, then all PL I/O banks can be tied to the same Vcco regulator.

A detailed discussion of the PL I/Os are available in the *PicoZed Hardware User Guide*. 
### 3.3 Analog

The Zynq XADC pins are connected through the MicroHeaders. For details of how this might be connected, see the MicroZed I/O Carrier Card User Guide and Schematics. Also, refer to Chapter 30 of the Zynq TRM, UG585, and UG480.

<table>
<thead>
<tr>
<th>Carrier Net Name</th>
<th>PicoZed 7010/7020 JX Connections</th>
<th>PicoZed 7015/7030 Pin#</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XADC_VP_0_P</td>
<td>JX1, pin 97</td>
<td>Bank 0, K9</td>
<td>XADC dedicated differential analog input</td>
</tr>
<tr>
<td>XADC_VP_0_N</td>
<td>JX1, pin 99</td>
<td>Bank 0, L10</td>
<td>Temperature-sensing diode pins</td>
</tr>
<tr>
<td>XADC_DXP_0_P</td>
<td>JX1, pin 98</td>
<td>Bank 0, M9</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_DXN_0_N</td>
<td>JX1, pin 100</td>
<td>Bank 0, M10</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD0_P</td>
<td>JX2, pin 17</td>
<td>Bank 35, C20</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD0_N</td>
<td>JX2, pin 19</td>
<td>Bank 35, B20</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD1_P</td>
<td>JX2, pin 23</td>
<td>Bank 35, E17</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD1_N</td>
<td>JX2, pin 25</td>
<td>Bank 35, D18</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD2_P</td>
<td>JX2, pin 36</td>
<td>Bank 35, M19</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD2_N</td>
<td>JX2, pin 38</td>
<td>Bank 35, M20</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD3_P</td>
<td>JX2, pin 35</td>
<td>Bank 35, L19</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD3_N</td>
<td>JX2, pin 37</td>
<td>Bank 35, L20</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD4_P</td>
<td>JX2, pin 54</td>
<td>Bank 35, J18</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD4_N</td>
<td>JX2, pin 56</td>
<td>Bank 35, H18</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD5_P</td>
<td>JX2, pin 68</td>
<td>Bank 35, J20</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD5_N</td>
<td>JX2, pin 70</td>
<td>Bank 35, H20</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD6_P</td>
<td>JX2, pin 73</td>
<td>Bank 35, K14</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD6_N</td>
<td>JX2, pin 75</td>
<td>Bank 35, J14</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD7_P</td>
<td>JX2, pin 82</td>
<td>Bank 35, L14</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD7_N</td>
<td>JX2, pin 84</td>
<td>Bank 35, L15</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD8_P</td>
<td>JX2, pin 18</td>
<td>Bank 35, B19</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD8_N</td>
<td>JX2, pin 20</td>
<td>Bank 35, A20</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD9_P</td>
<td>JX2, pin 29</td>
<td>Bank 35, E18</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD9_N</td>
<td>JX2, pin 31</td>
<td>Bank 35, E19</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD10_P</td>
<td>JX2, pin 41</td>
<td>Bank 35, M17</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD10_N</td>
<td>JX2, pin 43</td>
<td>Bank 35, M18</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD11_P</td>
<td>JX2, pin 42</td>
<td>Bank 35, K19</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD11_N</td>
<td>JX2, pin 44</td>
<td>Bank 35, J19</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD12_P</td>
<td>JX2, pin 62</td>
<td>Bank 35, F19</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD12_N</td>
<td>JX2, pin 64</td>
<td>Bank 35, F20</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD13_P</td>
<td>JX2, pin 67</td>
<td>Bank 35, G19</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD13_N</td>
<td>JX2, pin 69</td>
<td>Bank 35, G20</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD14_P</td>
<td>JX2, pin 81</td>
<td>Bank 35, N15</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD14_N</td>
<td>JX2, pin 83</td>
<td>Bank 35, N16</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD15_P</td>
<td>JX2, pin 88</td>
<td>Bank 35, K16</td>
<td>Differential auxiliary analog inputs</td>
</tr>
<tr>
<td>XADC_AD15_N</td>
<td>JX2, pin 90</td>
<td>Bank 35, J16</td>
<td>Differential auxiliary analog inputs</td>
</tr>
</tbody>
</table>

Table 8 - XADC Pinout
The XADC internal reference voltage is selected (VREFP and VREFN shorted AGND).

VCCADC is the on-board 1.8V filtered through a ferrite bead, with 0.1uF and 0.47uF bypass caps.

If you plan to make use of the XADC on your Carrier, it is suggested that you place anti-aliasing filters close to JX1 and JX2, similar to what is seen on the Microzed I/O Carrier Card. Be aware that the analog signal level is maximum 1Vpp. Please refer to Xilinx User Guide UG480.

When the XADC is not used, DXP/N, VP/N pins should be connected to GND. All the auxiliary analog inputs become digital I/O.

3.4 JTAG

The four dedicated JTAG signals are routed to the MicroHeaders. A Carrier Card must utilize these JTAG signals in order to program and debug with the PicoZed as a JTAG programming header is not implemented on board.

When connecting additional JTAG devices in-line with the PicoZed, be sure that TCK and TMS are properly buffered. For example, if you wanted to Device XYZ into the JTAG chain, you would design your Carrier Card with a PC4-socket, with TMS and TCK buffers after the socket. The buffered TMS and TCK would route to both Device XYZ and the MicroHeaders. Then the TDI/TDO connections would daisy-chain.

PC4 TDI ➔ JX1.4

JX1.3 ➔ Device XYZ TDI

Device XYZ TDO ➔ PC4 TDO

<table>
<thead>
<tr>
<th>PicoZed 7015/7030 Pin #</th>
<th>PicoZed 7010/7020 Pin #</th>
<th>Net Name</th>
<th>JX1 Pin #</th>
<th>JX1 Pin #</th>
<th>Net Name</th>
<th>PicoZed 7015/7030 Pin #</th>
<th>PicoZed 7010/7020 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank 0, H11</td>
<td>Bank 0, F9</td>
<td>JTAG_TCK</td>
<td>1</td>
<td>2</td>
<td>JTAG_TMS</td>
<td>Bank 0, J6</td>
<td>Bank 0, H10</td>
</tr>
<tr>
<td>Bank 0, G9</td>
<td>Bank 0, F6</td>
<td>JTAG_TDO</td>
<td>3</td>
<td>4</td>
<td>JTAG_TDI</td>
<td>Bank 0, G6</td>
<td>Bank 0, H9</td>
</tr>
</tbody>
</table>

Table 9 – JX1 Connections

3.5 Configuration

3.5.1 PUDC_B

This signal is the Pull-Up during Configuration signal. The net name on PicoZed 7010/7020 is JX1_LVDS_2_P. The net name on PicoZed 7015/7030 is JX2_LVDS_2_P. This signal has a resistor jumper option to pull-up to VCCO or pull-down to GND. The default is to pull it up via a 1K-ohm resistor, which disables the pull-ups during configuration.

This signal is routed to the Carrier. The default pull-up can be over-ridden with a stronger pull-down if pull-ups during configuration are desired.
3.5.2 DONE

The DONE signal is pulled-up on PicoZed via a 240-ohm resistor. The DONE signal is routed to the Carrier and can be used as a control input to signal when the PL is DONE configuring. It is recommended that the Carrier implement an LED to signal DONE is active.

<table>
<thead>
<tr>
<th>Function</th>
<th>Signal Name</th>
<th>MicroHeader Connection</th>
<th>Subsection</th>
<th>Zynq pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>PL Config DONE</td>
<td>FPGA_DONE</td>
<td>JX1.8</td>
<td>Bank 0</td>
<td>R11</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>T10</td>
</tr>
</tbody>
</table>

Table 11 – DONE

3.5.3 INIT_B

INIT_B is pulled-up via 4.7K-ohm on the PicoZed. If not needed as a controls signal on the Carrier, this can be left disconnected.

<table>
<thead>
<tr>
<th>Function</th>
<th>Signal Name</th>
<th>MicroHeader Connection</th>
<th>Subsection</th>
<th>PicoZed 7010/7020 Pin#</th>
<th>PicoZed 7015/7030 Pin#</th>
</tr>
</thead>
<tbody>
<tr>
<td>PL Initialization</td>
<td>INIT#</td>
<td>JX2.9</td>
<td>Bank 0</td>
<td>R10</td>
<td>T8</td>
</tr>
</tbody>
</table>

Table 12 – INIT_B

3.5.4 PROGRAM_B

PROGRAM_B is pulled-up via 4.7K-ohm on the PicoZed. For Zynq applications, it is not typical that a system would use this signal. The PicoZed does not provide connection to PROGRAM_B to the Carrier.

<table>
<thead>
<tr>
<th>Function</th>
<th>Signal Name</th>
<th>MicroHeader Connection</th>
<th>Subsection</th>
<th>PicoZed 7010/7020 Pin#</th>
<th>PicoZed 7015/7030 Pin#</th>
</tr>
</thead>
<tbody>
<tr>
<td>PL Program</td>
<td>PROGRAM#</td>
<td>none</td>
<td>Bank 0</td>
<td>L6</td>
<td>V10</td>
</tr>
</tbody>
</table>

Table 13 – PROGRAM_B
3.6 Ethernet MAC ID
From the factory, PicoZed does not store a MAC ID for the Ethernet. A designer could choose to implement this in the PicoZed Flash using their own MAC ID assignments.

A MAC ID could also be implemented using a dedicated MAC ID EEPROM, similar to what can be seen on the MicroZed FMC Carrier.

4 POWER AND RESET

4.1 General Power Requirements
The Carrier card provides system power to the PicoZed as well as providing power directly to the PL I/O banks on the Zynq device. The voltages that must be provided to PicoZed are listed below:

- **VIN** (PicoZed requires 5V)
- **VCCO_34** (Vcco for bank 34 on the Zynq device)
- **VCCO_35** (Vcco for bank 35 on the Zynq device)
- **VCCO_13** (Vcco for bank 13 on the Zynq device)
- **USB_VBUS_OTG** (USB 2.0 OTG 5V VBUS)
- **MGTAVCC** (Transceiver AVCC)
- **MGTAVTT** (Transceiver AVTT)

The total power budget is the power required for the carrier card (including the power supply inefficiencies) summed with the PicoZed power. This budget must include the anticipated current draw from the carrier card in “worst case” conditions, which is typically maximum I/O current sourcing, maximum data transfer rates across the high speed interfaces and a high temperature environment.

4.2 Power Estimation of PL using XPE
Refer to the *PicoZed Hardware Users Guide* for a detailed breakdown of the power requirements on the PicoZed. Xilinx Power Estimator (XPE) should be used to generate worst case power estimations for selecting power devices for the I/O banks. The Xilinx Power Estimator (XPE) spreadsheet is available on Xilinx’ website that can help you get started with your own power estimation. You may download this file and add or modify your desired PL utilization to provide a worst case estimation for your own VCCO supplies.

4.3 Proper Sequencing
All three Vccio banks that receive power from the Carrier can be independent, or tied together depending on the specific design needs. To maintain proper start up sequencing, these Vccio supplies should be enabled by the VCCIO_EN signal tied to JX2 pin 10. Note that this enable signal is the PGOOD from the 1.8V supply on PicoZed. It is vital to ensure that the enable threshold for the regulators chosen is compatible with a 1.8V signal. If 1.8V is not high enough to reliably enable the device, an external circuit must be used to boost this voltage. An example of such a circuit can be found in the schematic for the FMC Carrier card.
To enable power to the PicoZed, PWR_ENABLE must be pulled high. PWR_ENABLE is tied to JX1 pin 5 and is pulled up to VIN on the PicoZed. To shut down power to the PicoZed, PWR_ENABLE and VCCIO_EN should be pulled low. VCCIO_EN should be pulled low first to maintain proper shutdown sequencing.

4.4 Power Handling of PL I/O Banks and MGT Supplies
For designing the power supplies for the PL I/O banks and the MGTs, Xilinx Power Estimator (XPE) should be used to generate worst case power estimations. The Xilinx Power Estimator (XPE) spreadsheet is available on Xilinx’ website that can help you get started with your own power estimation. The power estimation results can then be used to budget for the power that will be needed by the PicoZed PL I/O banks and MGTs. This current should be added to the Carrier power estimate when designing your power system. The MGT Supplies are only necessary when planning a Carrier Card to support the PicoZed 7015/7030.

4.5 Proper Handling of VCCBAT
If battery backup is required, VCCBATT_0 must be tied to a 1.8V battery source through JX1 pin 7. Note that PicoZed by default ties VCCBATT_0 directly to 1.8V Vccaux. If using VCCBATT_0 as a battery backup, the 0-ohm resistor on VCCBATT_0 should be removed.

4.6 Proper Handling of XADC Power
The XADC interface operates from a 1.8V supply voltage with a 1.25V reference. Be sure to design your interface with these values in mind. Do not exceed 1.8V on the XADC inputs. For additional information on designing with this interface please refer to Xilinx Application Note XAPP554 – XADC Layout Guidelines.

4.7 Need for Additional Bypass Capacitors
Bulk and decoupling/bypass capacitance is provided on PicoZed. Additional capacitance should be added to the user designed Carrier as recommended by the device manufacturers for each interface.
5  CARRIER BOARD PCB GUIDELINES

The majority of the PicoZed PL signals are routed to the JX connectors to facilitate user design flexibility and application development. Differential pairs and single ended signals are available for custom carrier card designs. All high speed routing must follow the specific device manufacturers’ recommendations for routing, impedance, trace length and layout guidelines. This is applicable to any high speed or low noise signals such as DDR RAM, Ethernet PHY, PMODs, XADC or USB extensions. The design engineer must be diligent in these areas to ensure intended data rates and performance.

The specific design requirements for a user application will ultimately drive the trace-length, trace spacing, signaling topology (differential or single ended) and impedance requirements. This variability cannot be accounted for and data throughput, signal integrity and overall performance will vary based on the design approach.

In all circumstances the design of a user Carrier board, the following documents should be consulted and adhered to: PicoZed User Guide, the PicoZed Carrier Card User Guide, and Xilinx’s UG430. These documents provide critical insight into how the Avnet products were designed.

For general guidelines on how to achieve the performance of the Avnet Carrier Card designs, Avnet Engineering Services suggests the following design requirements be adhered to.

5.1  Suggested Requirements for Optimum Carrier Card Performance

5.1.1  Global Target Impedances (Unless otherwise noted)
– 100Ω differential impedance
– 50Ω single ended impedance
– USB: 45Ω single ended, 90Ω differential
– DDR: 40Ω single ended, 80Ω differential

5.1.2  Pair Matching and Length Tuning
– Use 4x spacing between pairs
– All signals should be routed using stripline or microstrip techniques.
– Length tune all signal pairs to within 10 mils within each pair (P to N)
– Length tune all signal pairs to within 250 mils pair-to-pair (depending on transfer rates)
– For high speed interfaces such as DDR memory Zynq internal package flight delays should be considered. Package flight delays for specific parts and packages can be obtained from the Vivado design tool. For package flight tolerances specific to DDR interfaces refer to Xilinx document UG586 Chapter 1.
– Both PicoZed 7010/7020 and PicoZed 7015/7030 length tune all of the traces between the Zynq and the JX1/JX2 connectors to be equal. Each connector is treated as a separate interface. Please refer to Appendix A for the actual routed net lengths on the PicoZed SOMs.

5.1.3  Routing Considerations for Additional DDR Modules (PL via JX Connectors)
– LPDDR2, DDR2, and DDR3 should be selected based on MIG tool for a Zynq processor.
– Use the MIG tool pin-out information to route from the JX1 and JX2 connectors on the carrier board.
– Place memory IC (or ICs), pending topology and memory density, as close as possible to the JX1 and JX2 Microheaders for maximum data transfer rates and to minimize long trace lengths.
– Follow specific memory manufacturer’s routing guidelines, trace impedance requirements and termination topology. The PicoZed uses a 40Ω ohm single ended and 80Ω differential trace impedance for the specific DDR3 with a 3X spacing between pairs, matching the memory manufacturer’s recommendations.
– Routing, impedance and termination requirements will vary depending on the memory manufacture, the quantity of DDR ICs, the topology and the desired data throughput performance.
– As a general rule for high speed memory, Avnet adheres and recommends memory trace lengths to be less than 5000 mil in total length.
– All memory signals should be length tuned according to total propagation delay or “flight time” as recommended by Xilinx and the chosen memory manufacturer.
– Avnet recommends routing all memory signals on inner layers only, within 10mils of each other pair to pair, less than 50mils for a byte-lane associated to each DQS, and all memory signals to be within 100 mils of each other.

5.2 Routing 1Gb/s Ethernet and USB Through the PL
– Using Vivado IP integrator or ISE Core Generator, develop a MAC interface for the Zynq PL.
– All Giga-bit signals should be routed stripline using micro-vias between the appropriate layers.
– Use 4x spacing between pairs.
– Single pair (P and N) should be length tuned to within 25 mils of each other (P to N) at 100Ω differential impedance, with no more than two transitions (vias) for these signals.
– All Data, clock and control signals should be routed at 50Ω impedance and not exceed the PHY manufacturers’ recommended length requirements.
– All interface signals should be routed to within 250mils of each other.
– If RGMII interface is used, the related VCCO must supply 1.8V or 2.5V to support fast slew.
– The Ethernet PHY must be compatible with VCCO levels used.

5.3 Routing MGTs on the Carrier Card
It is highly suggested that the guidelines described in the Xilinx document(s) “7-Series FPGAs GTP Transceivers” (UG482) Chapter 5 and “7-Series FPGAs GTX/GTH Transceivers User’s Guide” (UG476), Chapter 5 be reviewed prior to designing and routing GTP/GTX circuits.

Here are some general guidelines that are followed on the SOMs’ GTP/GTX routing:
– All gigabit transceiver signals shall be routed Stripline.
– All gigabit transceiver TX, RX and related clock differential signals shall be routed differential at 100 ohms differential impedance.
– Use 4x spacing between pairs.
– All gigabit transceiver signals shall be length tuned to within 100 mils shortest pair to longest pair.
– All gigabit transceiver signals within a single pair (P and N) shall be length tuned to within 25 mils of each other (P to N).
– No more than two transitions (vias) are allowed for these signals.
5.4 Routing AMS/XADC Signals

The XADC header provides analog connectivity for analog reference designs, including AMS daughter cards such as Xilinx’s AMS Evaluation Card. Both analog and digital IO can be easily supported for a plug in card.

The pin out has been chosen to provide tightly coupled differential analog pairs on the ribbon cable and to also provide AGND isolation between channels.

To minimize signal aliasing, the following filters should be used for the XADC inputs:

- VP/VN
- VAUX0P/VAUX0N
- VAUX8P/VAUX8N

![Figure 3 – Anti-Aliasing Filters for XADC Inputs](image)

- The 100Ω filtering resistors and 1000pF capacitor should be placed within 500 mils of the associated FPGA pins.
- Use 4X spacing on the traces.
- Single ended impedance is 50Ω and differential is 100Ω.
- All paired signals should be routed to within 50mils of each other.
- All interface signals should be routed to within 100mils of each other.
- Anti-aliasing filters should be placed as close to the MicroHeader as possible.

5.4.1 XADC alternate GPIO function

If the XADC function is not desired, the port can be used for additional GPIO expansion as necessary. However, care must be taken to ensure the appropriate logic voltage levels are observed when using these signals. VCCIO_35 sets the acceptable voltage levels for the XADC_GPIOx signals. For AD*_P/N signals must be limited to 1.8V logic levels.

To facilitate a high performance interface, the suggested layout guidelines should be followed.
6 PICOZED CONNECTORS
Each PicoZed SOM features three 100-pin MicroHeaders (JX1, JX2, and JX3) that allow for connection to customer Carrier cards. The MicroHeaders route I/O signals and power between PicoZed and a custom carrier card.

6.1 Connector Description and Selection
The MicroHeaders used on PicoZed are FCI 0.8mm BergStak® 100-position Dual Row, BTB Vertical Receptacles (61082-101400LF). These receptacles mate with any of the FCI 0.8mm BergStak® 100-position Dual Row BTB Vertical Plugs (61083-10x400LF) to provide variable stack heights of 5mm, 6mm, 7mm or 8mm. See table below for additional detail.

Custom PicoZed modules can be ordered with specific receptacles while custom carrier cards can be populated with specific plugs allowing system designers to choose optimal stacking heights (5mm – 16mm in 1mm increments) for their particular application. See table below for additional detail.

![Figure 4 - FCI BergStak Mating Options](image-url)
Additionally, each MicroHeader pin can carry 500mA of current and can support data rates up to 8Gbps. More information on FCI’s BergStak connectors can be found at www.fciconnect.com/bergstak.

Avnet will keep the following FCI part numbers in Table 12 in stock to assist prototype build of custom carrier cards. See www.em.avnet.com/avnetsomconnectors for more details.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>61082-10140xLF*</td>
<td>61083-10140xLF*</td>
</tr>
<tr>
<td>61082-10240xLF*</td>
<td>61083-10240xLF*</td>
</tr>
<tr>
<td>61082-10340xLF*</td>
<td>61083-10340xLF*</td>
</tr>
<tr>
<td></td>
<td>61083-10440xLF*</td>
</tr>
</tbody>
</table>

Table 14 - FCI BERGSTAK Connectors

* “x” can be 0, 2 or 9 depending on packaging.

Avnet will keep the following FCI part numbers in Table 12 in stock to assist prototype build of custom carrier cards. See www.em.avnet.com/avnetsomconnectors for more details.

6.1.1 Connector Shock and Vibration Specifications

Shock:

EIA-364-27, Test Condition A

Accelerated velocity ----- 490 m/s² (50G).

Waveform --------------- half-sine shock pulse.

Duration --------------- 11 mSec.

Velocity change --------- 11.3 feet per second

Number of cycles ------- 18

Vibration:

EIA-364-28 Test Condition V, Letter D

Frequency ------------------ 50 to 2000 Hz

Power spectral Density ------ 0.1 g²/Hz

Overall rms g ------------------ 11.95

Duration --------------------- 1 1/2 hours in each of three mutually perpendicular axes (4 1/2 hours total).
### 6.2 MicroHeader Pinouts

<table>
<thead>
<tr>
<th>PicoZed 7015/7030 Pin #</th>
<th>PicoZed 7010/7020 Pin #</th>
<th>Net Name</th>
<th>JX1 Pin #</th>
<th>JX1 Pin #</th>
<th>Net Name</th>
<th>PicoZed 7010/7020 Pin #</th>
<th>PicoZed 7015/7030 Pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 – H11</td>
<td>0 - F9</td>
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Table 17 – JX3 Connections
Page 26
6.3 Connector Land and Alignment

It is extremely important that Carrier card designers ensure that the MicroHeaders have the proper land patterns and that the connectors are aligned correctly. The land pattern is featured in the *Mechanical Considerations* section of this document. Connector alignment is ensured if the alignment pin holes in the PCB connector pattern are in the correct positions and if the holes are drilled to the proper size and tolerance by the PCB fabricator.

If a customer would like a template for laying out their custom board, Avnet-qualified customers can request the source through their local Avnet FAE.
7 MECHANICAL CONSIDERATIONS

PicoZed measures 2.25” x 4.00” (57.15 mm x 101.6 mm). Custom carrier cards would have to be large enough to support the dimension shown below. Figure 3 is referenced as the footprint on a customer carrier card top view.

PicoZed comes with four grounded and plated mounting holes in each of the four corners of the board. The diameter of each mounting hole is 0.125” (3.175mm). Assuming the standard 5mm board-to-board spacing between PicoZed and the carrier card, spacers (i.e. Harwin R30-3000502 with M3x5mm metal screw and M3 x 1mm metal nut) can be added to mechanically strengthen the attachment of PicoZed to the Carrier card. Metal standoffs provide an additional heat dissipation path for any possible heat buildup on the ground layer.

PicoZed 7010/7020 comes with two un-plated mounting holes near the Zynq device. The diameter of each mounting hole is 0.093” (2.362mm). These can be used to secure thermal relief elements like fans or a heat spreader. M2 diameter screws, spacers and nuts can be used on the mounting holes. See the following figures for more detail. PicoZed 7015/7030 does not have mounting holes near the Zynq device and would require a thermal adhesive to mount thermal relief elements.
7.1 Form Factor

Figure 5 - Mechanical Layout of PicoZed Carrier Card
MicroHeader Connectors and Mounting Holes

7.2 Thermal Considerations

Thermal relief is an important design factor in each PicoZed-based system design. A detailed thermal analysis should be performed for each specific application of PicoZed and a customer designed carrier card. In support of this, PicoZed has many design features to help dissipate heat from a system level.

The first feature is the fan header. This header provides two ground connections and one connection to the $V_{IN}$ voltage (3.3V or 5V Selectable). This allows a fan to be added to any PicoZed-based system. For maximum heat dissipation, any system airflow should pass parallel to the surface of the Zynq.

Related to the fan header are two mounting holes located next to the Zynq 7010/7020 device. This allows for a fan, heat sink or fan and heatsink combination to be added to the PicoZed 7010/7020. System engineers may decide to mount a heat spreader here in extreme situations. The Zynq
7015/7030 does not contain these mounting holes and any thermal solution would be required to adhere to the Zynq device.

Lastly, the four mounting holes on the four corners of PicoZed are electrically connected to a heavier ground plane. With the additional mounting holes added to PicoZed, system designers may choose to attach PicoZed to their customer carrier card using metal standoff providing another path for heat dissipation.

In some instances adding a passive heat sink with appropriate thermal bonding material to the Zynq may be sufficient to dissipate any extra heat. The Zynq package used on PicoZed 7010/7020 measures 17mm by 17mm or 19mmx19mm for the PicoZed 7015/7030. For maximum heat transfer, passive heat sinks attached to the Zynq device should cover the entire area. Suggested devices below serve as a starting point for basic heat dissipation needs.

<table>
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<tr>
<th>Manufacturer</th>
<th>Part Number</th>
<th>L x W X H (mm)</th>
<th>Thermal Resistance (°C/W)</th>
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<td>19 x 19 x 6.3</td>
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Table 18 – PicoZed Heatsink Options

*@200LFM
8 GETTING HELP AND SUPPORT
If additional support is required, Avnet has many avenues to search depending on your needs.

For general question regarding PicoZed and PicoZed Carrier Card or accessories, please visit our website at http://www.picozed.org. Here you can find documentation, technical specifications, videos and tutorials, reference designs and other support.

Detailed questions regarding PicoZed hardware design, software application development, using Xilinx tools, training and other topics can be posted on the PicoZed Support Forums at http://www.picozed.org/forums/zed-english-forum. Avnet’s technical support team monitors the forum during normal business hours.

Those interested in customer-specific options on PicoZed can send inquiries to customize@avnet.com.

Avnet’s Embedded Software Store addresses the need for software in the embedded architecture development space. The goal of this store is to provide a market place for engineers to easily purchase software components for given hardware architectures. Support for the Xilinx Zynq AP SoC includes Board Support Packages, Middleware, Operating Systems and various tools.

The Embedded Software and Services Group (ESSG) of Avnet Embedded offer a suite of software services that optimize the entire embedded software stack. Flexible end-to-end solutions enhance operating systems, middleware, application layers and cloud solutions based on the embedded system needs. More information can be found at http://www.em.avnet.com/en-us/services/Pages/Software-Solutions.aspx.
## APPENDIX A – SOM JX1/JX2 Routed Net Lengths

### JX1

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Table 19 – PicoZed 7010/7020 JX1/JX2 Net Lengths

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Table 20 – PicoZed 7015/7030 JX1/JX2 Net Lengths