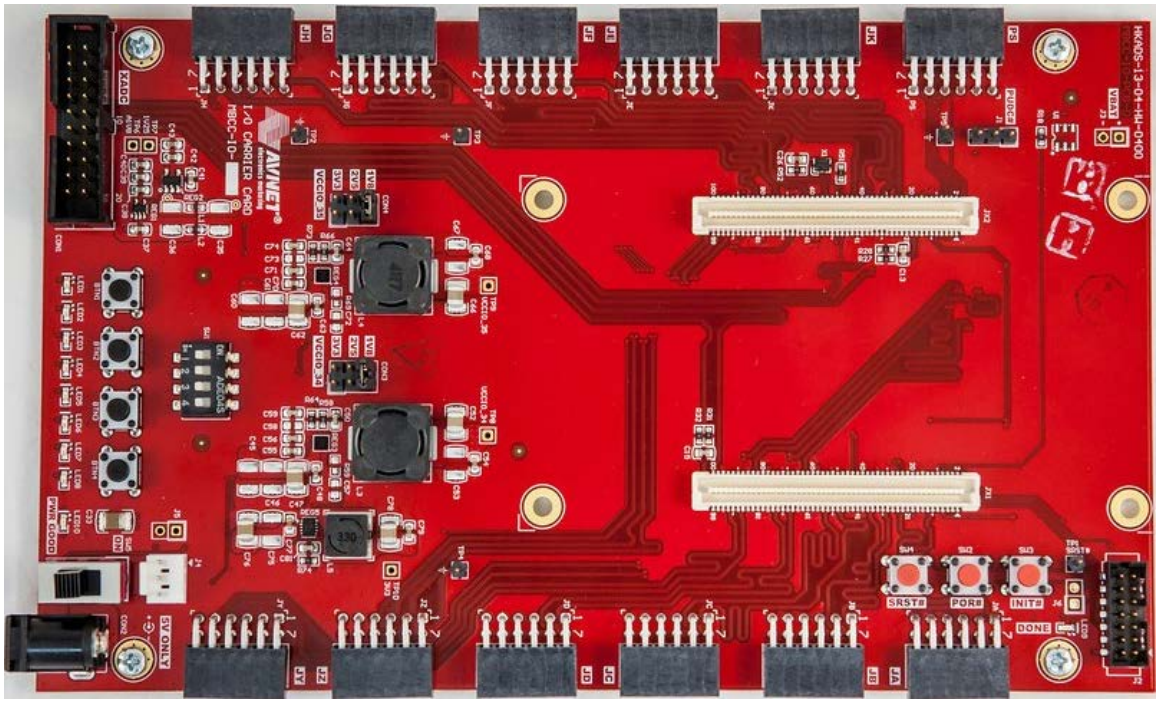
MicroZed I/O Carrier Card

Zynq™ System On Module
Hardware User Guide



Revision 1.3
26 Aug 2014

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1 Introduction

The MicroZed I/O Carrier Card (IOCC) is a low cost evaluation board for the MicroZed series System On Module (SOM) boards. The function of this board is to provide SoC I/O pin accessibility to the MicroZed SOM board through the 12 PMOD connectors. In addition to SoC I/O pin access through the PMOD connectors, the IOCC also provides SOM board power via the JX MicroHeaders. Please refer to the MicroZed Hardware User's guide for the MicroZed's feature set. The features provided by the IOCC consist of:

- Interfaces
  - Xilinx PC4 Header for programming
    - Accesses PL JTAG
  - 12 Digilent Pmod™ compatible interfaces
    - One connected to PS MIO
    - Two connected to Bank 13 PL (MicroZed with Zynq 7Z020 only)
    - Five connected to Bank 34 PL
    - Four connected to Bank 35 PL
  - Two 100-pin MicroHeaders
  - Reset Push Button
  - 4 User Push Buttons
  - 2 Configuration Push Buttons
  - 8 User LEDs
  - 4 User DIP Switches
  - 2 Status LEDs
  - Xilinx XADC Header

- On-board Oscillator:
  - 100MHz single ended with FPGA control

- On-board Memory:
  - Optional footprint: 1KB 1-wire SHA Security EEPROM (not populated)

- Power
  - Internal
    - Filtered Vin for XADC (5V only).
    - 85%+ high-efficiency regulators for 1.8V/2.5V/3.3V @ 2.3A
      - For Module VCC_{IO} Bank_34
    - 85%+ high-efficiency regulators for 1.8V/2.5V/3.3V @ 2.85A
      - For Module VCC_{IO} Bank_35 and Bank 13 (7Z020 only)
    - Low Noise LDO 1.8V @ 0.15A supply for XADC
    - 0.2% accurate 1.25V @ 0.05A precision reference for XADC

  - External
    - Primary 5V ≥ 2.0 A

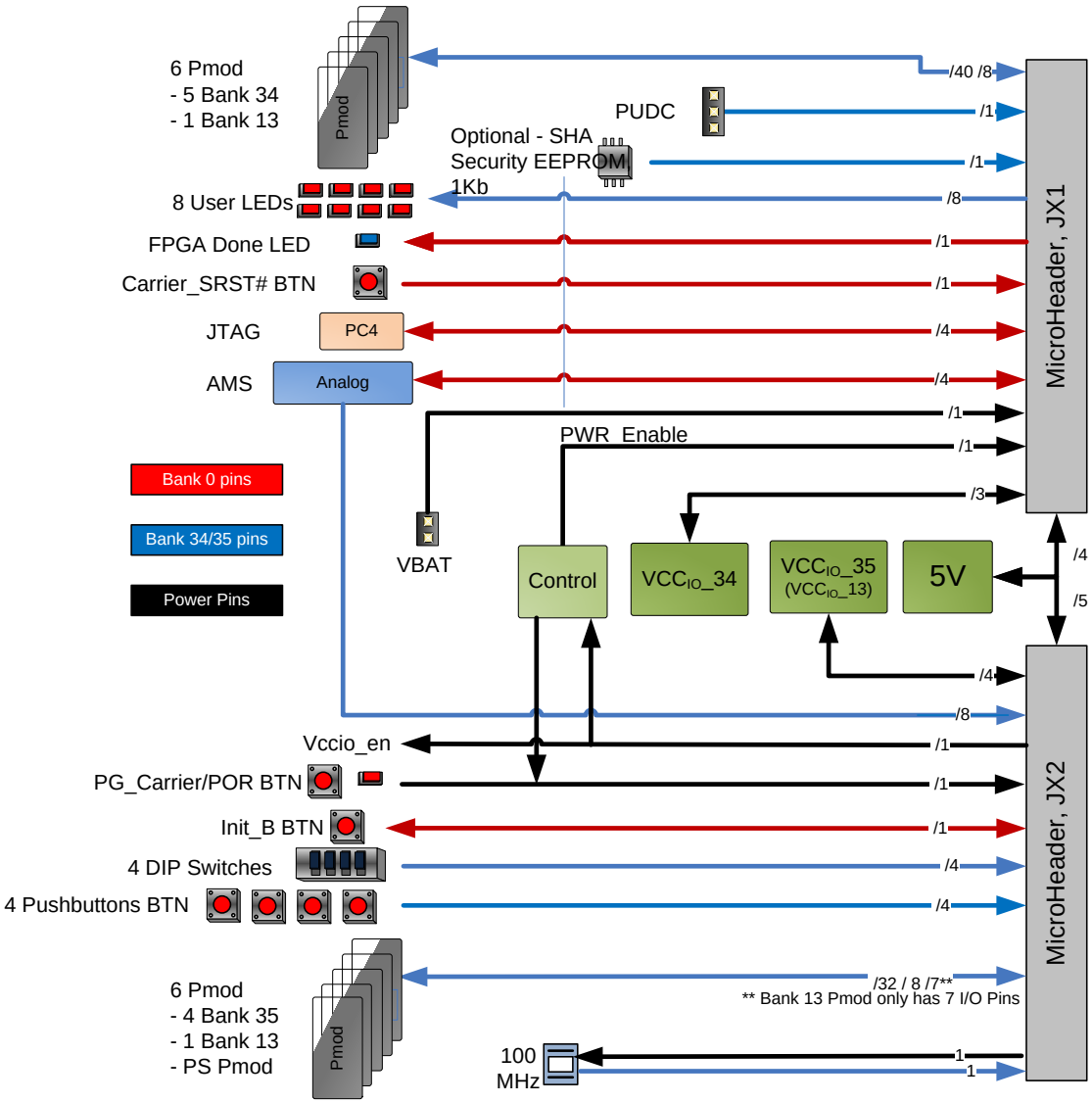

Figure 1 – MicroZed IOCC Block Diagram

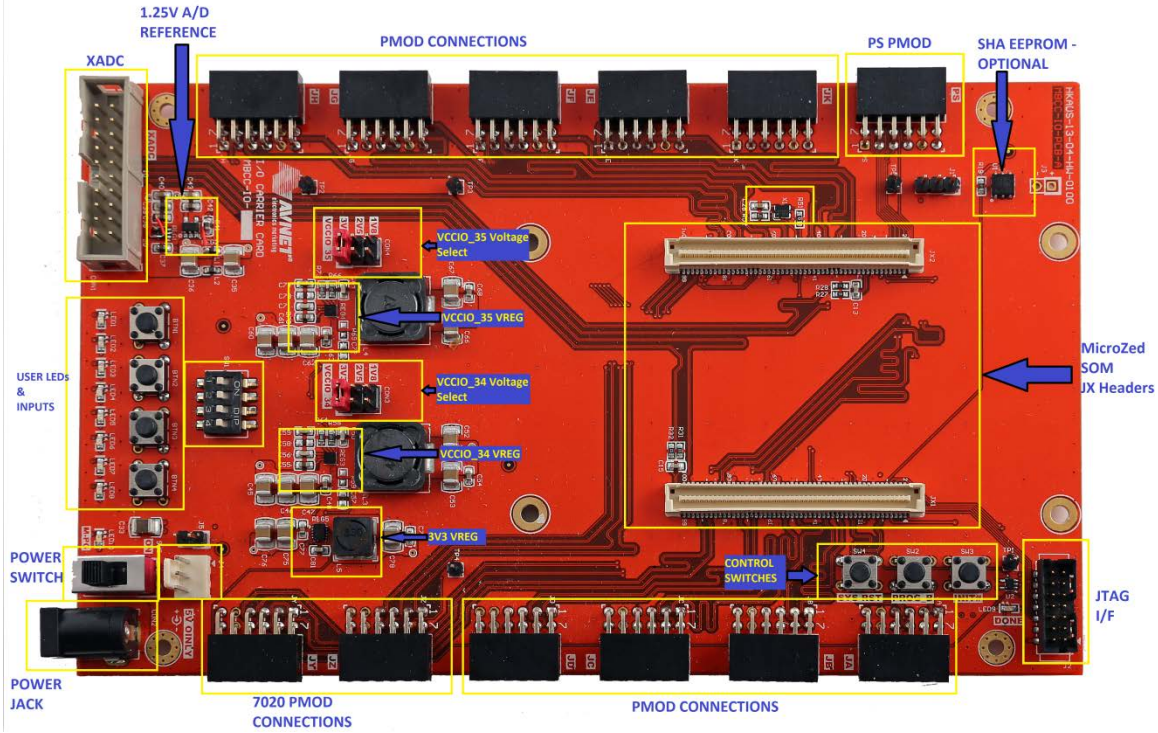

Figure 2: IOCC Topology

1.1 Zynq Bank Pin Assignments

The following figure shows the Zynq bank pin assignments on the MicroZed followed by a table that shows the detailed I/O connections. See tables Table 12 – JX1 Connections and Table 13 – JX2 Connections.

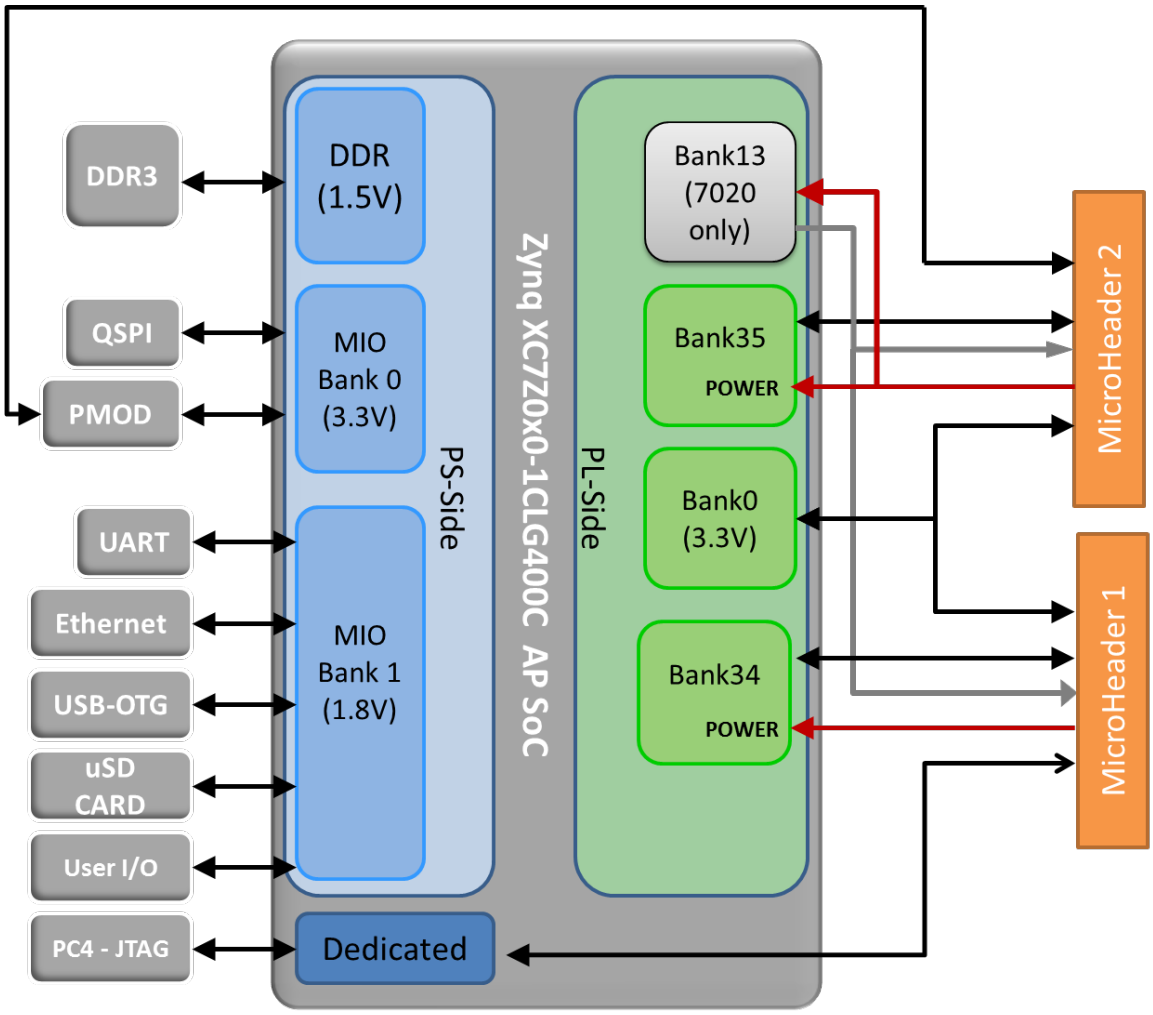

Figure 3 – Zynq CLG400 Bank Assignments

2 Functional Description

The I/O Expansion Carrier Card is an expansion board for Avnet's MicroZed 7Z010 or 7Z020 System On Module (SOM) product. It adds up to 12 Digilent Pmod™ compatible Interfaces, 8 User LEDs, 4 User Pushbuttons, 4 DIP Switches and a Xilinx analog interface.

2.1 Memory – 1Kb SHA Security EEPROM – optional

The Carrier features a footprint for a Maxim 1-Wire SHA-1 Authenticated 1Kb EEPROM, DS28E02P+. The DS28E02 combines 1024 bits of EEPROM with challenge-and-response authentication security implemented with the FIPS 180-3 Secure Hash Algorithm (SHA-1).

The 1024-bit EEPROM array is configured as four pages of 256 bits with a 64-bit scratchpad to perform write operations. All memory pages can be write protected, and one page can be put in EPROM-emulation mode, where bits can only be changed from a 1 to a 0 state. Each DS28E02 has its own guaranteed unique 64-bit ROM registration number that is factory installed into the chip.

The DS28E02 communicates over the single-contact 1-Wire® bus. The communication follows the standard 1-Wire protocol with the registration number acting as the node address in the case of a multidevice 1-Wire network. Pin 2 of this device must be pulled high with a 680ohm resistor to VCCio_34.

Table 1 – SHA EEPROM Connection

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection
1W-EEPROM	JX1.10	JX_SE_1

2.2 Clock source

A 100 MHz single ended clock is attached to one of the MRCC pins in PL bank 35, allowing it to connect directly to internal MMCM's and PLL's of the Zynq AP SOC. The FPGA enables this clock via the BB_CLK_EN signal. Default power on state for this clock is pulled down, thereby off.

Table 2 – 100 MHz Clock Connection

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection
BB_CLK	JX2.48	JX2_LVDS_11_P
BB_CLK_EN	JX2.50	JX2_LVDS_11_N

2.3 Reset sources

2.3.1 INIT# button – SW3

The INIT# button provides an active low input signal to the FPGA. It is used to stall the power-on configuration sequence at the end of the initialization process of the FPGA. This signal is rarely used.

Table 3 – INIT# Connection

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection
INIT#	JX2.9	INIT#

2.3.2 Power On Reset – POR# button – SW2

The POR# button provides an active low signal to the PG_CARRIER net on the JX2 MicroHeader. When asserted, this signal resets the USB UART, USB OTG circuit and turns off the IOCC VCCIO_34/35 power supplies. It is used to invoke an IOCC and MicroZed total system power reset. The PS and PL are reset to power on default settings and the selected boot process is initiated.

Table 4 – POR Connection

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection
PG_CARRIER	JX2.11	PG_MODULE

2.3.3 Processor Subsystem Reset: SYS_RST# button – SW4

The SYS_RST# button provides and active low signal to net CARRIER_SRST# which allows the user to reset all of the functional logic within the device without disturbing the debug environment. For example, the previous break points set by the user remain valid after system reset. Due to security concerns, system reset erases all memory content within the PS, including the OCM. The PL is also reset in system reset. System reset does not re-sample the boot mode strapping pins.

Table 5 – SYS_RST# Connection

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection
CARRIER_SRST#	JX1.6	CARRIER_SRST#

2.4 User I/O

2.4.1 User Push Buttons

The Carrier provides 4 user GPIO push buttons to the Zynq-7000 AP SoC.. Pull-down resistors provide a known low default state. Pushing a button connects to VCCio_35 to assert a logic high.

Table 6 – Push Button Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection
PB0	JX2, pin 67	Bank 35, G19
PB1	JX2, pin 69	Bank 35, G20
PB2	JX2, pin 68	Bank 35, J20
PB3	JX2, pin 70	Bank 35, H20

2.4.2 User LEDs

The Carrier has 8 user LEDs. A logic high from the Zynq-7000 AP SoC I/O turns the LED on. LED's are sourced from VCCio_34, banks through current limiting resistors.

*Note, if VCCio_34 is set to 1.8V, the LED intensity will be noticeably lower than when VCCio_34 is set to 3.3V.

Table 7 – LED Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection
LED0	JX1, pin 41	Bank 34, U14
LED1	JX1, pin 43	Bank 34, U15
LED2	JX1, pin 42	Bank 34, U18
LED3	JX1, pin 44	Bank 34, U19
LED4	JX1, pin 9	Bank 34, R19
LED5	JX1, pin 19	Bank 34, V13
LED6	JX1, pin 24	Bank 34, P14
LED7	JX1, pin 26	Bank 34, R14

2.4.3 DIP Switches

The 4 user-selectable DIP switches are pulled down (low) in the OFF position. In the ON position they are connected to VCCio_35.

Table 8 – User Switch Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection
DIP_SW0	JX2, pin 87	Bank 35, M14
DIP_SW1	JX2, pin 89	Bank 35, M15
DIP_SW2	JX2, pin 88	Bank 35, K16
DIP_SW3	JX2, pin 90	Bank 35, J16

2.5 Interface Headers

2.5.1 Digilent Pmod™ Compatible Expansion Headers (2x6)

The Carrier has 12 Digilent Pmod™ right angle 0.1" female headers (2x6). These connections include eight user I/O plus an adjustable voltage derived from VCCIO_34 and VCCIO_35 power supplies. These power supplies are jumper selectable to provide 1.8V, 2.5V or 3.3V. When 3.3V is selected, the connectors are Pmod compatibale. All Pmod™ connections with the exception of the PS Pmod™ are matched differential Pmod™ connections and are routed differentially within the connector and with reference to one another to ensure high speed signal integrity.

- The Digilent Pmod™ compatible interface connects to Zynq banks 500, 34, 35 and 13. Bank 13 is only available on the 7Z020 version MicroZed.

- The PS Pmod attached to bank 500 can be used for PJTAG access (MIO[10-13]) as well as utilizing nine other hardened MIO peripherals (SPI, GPIO, CAN, I2C, UART, SD, QSPI, Trace, Watchdog). NOTE: The PS Pmod™ is also accessible on MicroZed and only can be used by one Digilent Pmod™ compatible interfaces at one time. The PS Pmod is 3.3V only.

- 7Z020 MicroZed only: Pmods™ ,JY and JZ, are sourced by Bank 13 and thus only available when MicroZed is populated with a 7Z020 device. Pmod™ JZ only has 7 pin connections, thus this Pmod™ interface cannot interface to QSPI or SD interface per the Digilent Pmod™ specification.

- There is an XDC constraints file for the MicroZed IO Carrier Card available for download on the MicroZed IO Carrier Card documentation page at www.microzed.org.

Figure 4 – Digilent Compatible Pmod™ Interface Layout

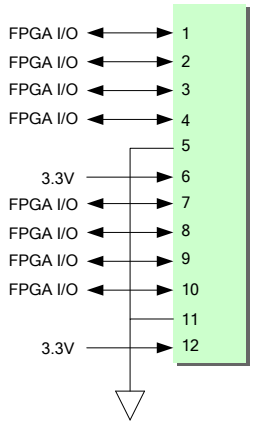

Figure 5 – Digilent Pmod™ Compatible Interface Connections when VCCIO_34/35 set to 3.3V.

2.5.2 JX1 and JX2 MicroZed interface microheaders

The Carrier features two MicroHeaders (TE PN: 5177984-4) for connection to MicroZed. Each connector interfaces to Zynq PL I/O as well as eight PS-GPIO, six dedicated analog inputs, and four dedicated JTAG signals.

***NOTE:** the eight PS-GPIO and four JTAG signals are shared on MicroZed, thus for each interface, it can only be used on either MicroZed or the Carrier, not simultaneously.

- The connectors are FCI BERGSTAK 0.8mm pitch. These have variable stack heights from 5mm to 20mm, making it easy to connect to a variety of expansion or system boards.

- Each connector has 100 pins which include I/O, analog signals, as well as power and ground. The Carrier powers the MicroZed as an alternative to the USB-UART. Each pin can carry 500mA of current and has been tested and certified against PCIe Gen2, thus sufficient bandwidth for this interface.

- MicroZed does not power the PL VCC_{IO} banks, this is required by the Carrier. This gives the Carrier the flexibility to control the I/O bank voltages. The 7Z010 has two PL I/O banks, banks 34 and 35, each containing 50 I/O.

- The 7Z020 has a third I/O bank, bank 13, which is powered on the IOCC by the same supply as Bank35.

- Within a PL I/O bank, there are 50 I/O capable of 24 differential pairs. Differential LVDS pairs on a -1 speed grade device are capable of 950Mbps of DDR data. Each differential pair is isolated by a power or ground pin. Additionally, eight of these I/O can be connected as clock inputs (four MRCC and four SRCC inputs).

- Each PL bank can also be configured to be a memory interface with up to four dedicated DQS data strobes and data byte groups. Bank 35 adds the capability to use the I/O to interface up to 16 differential analog inputs. One of the differential pairs in Bank 34 is not used as one of the pins is shared with PUDC_B.

- The MicroZed with the Zynq 7Z020 populated has bank 13. While the bank has 25 I/Os, only 15 of these signals are routed to the MicroHeader due to the header's pin limitations.

Table 9 – Bank 13 Pins

Number of Pins	Name	Pin Number
1**	VCCO_13	T8 U11 W7 Y10
1	IO_L6N_T0_VREF_13	V5
2	IO_L12P_T1_MRCC_13 IO_L12N_T1_MRCC_13	T9 U10
2	IO_L11P_T1_SRCC_13 IO_L11N_T1_SRCC_13	U7 V7
2	IO_L15P_T2_DQS_13 IO_L15N_T2_DQS_13	V8 W8
8 (Byte Group T3)	IO_L19P_T3_13 IO_L19N_T3_VREF_13 IO_L20P_T3_13 IO_L20N_T3_13 IO_L21P_T3_DQS_13 IO_L21N_T3_DQS_13 IO_L22P_T3_13 IO_L22N_T3_13	T5 U5 Y12 Y13 V11 V10 V6 W6

** With only one pin for VCCO_13, the PCB trace must be able to carry 500mA.

2.5.2.1 MicroHeader pinout assignments:

Table 10 – MicroHeader Pinout

MicroHeader #1				MicroHeader #2			
Signal Name		Source	Pin Count	Signal Name		Source	Pin Count
PL	All Bank 34 Pins	Zynq Bank 34	49	PL	All Bank 35 Pins	Zynq Bank 35	50
JTAG	TMS_0	Zynq Bank 0	5	PS	PS Pmod MIO[0,9-15]	Zynq Bank 500	8
	TDI_0	Zynq Bank 0		C	Init_B_0	Zynq Bank 0	2
	TCK_0	Zynq Bank 0			Program_B_0	Zynq Bank 0	
	TDO_0	Zynq Bank 0		Power	PG_Module	Module	1
	Carrier_SRST#	Carrier			5V	Carrier	28
Analog	VP_0	Zynq Bank 0	4		GND	Carrier	
	VN_0	Zynq Bank 0			VCCO_35	Carrier	3
	DXP_0	Zynq Bank 0			Bank 13 pins	Bank 13 **	8
	DXN_0	Zynq Bank 0			**Total**		10
C	PUDC_B	Zynq Bank 34	2				
	DONE	Zynq Bank 0					
Power	PWR_Enable	Carrier	1				
	Power	Carrier	28				
	GND	Carrier					
	VCCO_34	Carrier	3				
	Bank 13 pins	Bank 13 **	8				
TOTAL			100				

** 7020 device only

Table 11 – JX1 Connections

Carrier Connection	Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection	Zynq AP SOC Pin
XADC, pin 1	XADC_V_N	JX1, pin 99	Bank 0, K9	VN_0
XADC, pin 2	XADC_V_P	JX1, pin 97	Bank 0, L10	VP_0
XADC, pin 9	XADC-DX_P	JX1, pin 98	Bank 0, M9	DXP_0
XADC, pin 12	XADC-DX_N	JX1, pin 100	Bank 0, M10	DXN_0
LED0	LED0	JX1, pin 41	Bank 34, U14	IO_L11P_T1_SRCC_34
LED1	LED1	JX1, pin 43	Bank 34, U15	IO_L11N_T1_SRCC_34
LED2	LED2	JX1, pin 42	Bank 34, U18	IO_L12P_T1_MRCC_34
LED3	LED3	JX1, pin 44	Bank 34, U19	IO_L12N_T1_MRCC_34
LED4	LED4	JX1, pin 9	Bank 34, R19	IO_0_34
LED5	LED5	JX1, pin 19	Bank 34, V13	IO_L3N_T0_DQS_34
LED6	LED6	JX1, pin 24	Bank 34, P14	IO_L6P_T0_34
LED7	LED7	JX1, pin 26	Bank 34, R14	IO_L6N_T0_VREF_34
Pmod JA, pin 1	JA0-1 P	JX1, pin 11	Bank 34, T11	IO_L1P_T0_34
Pmod JA, pin 2	JA0-1 N	JX1, pin 13	Bank 34, T10	IO_L1N_T0_34
Pmod JA, pin 3	JA2-3 P	JX1, pin 12	Bank 34, T12	IO_L2P_T0_34
Pmod JA, pin 4	JA2-3 N	JX1, pin 14	Bank 34, U12	IO_L2N_T0_34
Pmod JA, pin 7	JA4-5 P	JX1, pin 18	Bank 34, V12	IO_L4P_T0_34
Pmod JA, pin 8	JA4-5 N	JX1, pin 20	Bank 34, W13	IO_L4N_T0_34
Pmod JA, pin 9	JA6-7 P	JX1, pin 23	Bank 34, T14	IO_L5P_T0_34
Pmod JA, pin 10	JA6-7 N	JX1, pin 25	Bank 34, T15	IO_L5N_T0_34
Pmod JB, pin 1	JB0-1 P	JX1, pin 29	Bank 34, Y16	IO_L7P_T1_34
Pmod JB, pin 2	JB0-1 N	JX1, pin 31	Bank 34, Y17	IO_L7N_T1_34
Pmod JB, pin 3	JB2-3 P	JX1, pin 30	Bank 34, W14	IO_L8P_T1_34
Pmod JB, pin 4	JB2-3 N	JX1, pin 32	Bank 34, Y14	IO_L8N_T1_34
Pmod JB, pin 7	JB4-5 P	JX1, pin 35	Bank 34, T16	IO_L9P_T1_DQS_34
Pmod JB, pin 8	JB4-5 N	JX1, pin 37	Bank 34, U17	IO_L9N_T1_DQS_34
Pmod JB, pin 9	JB6-7 P	JX1, pin 36	Bank 34, V15	IO_L10P_T1_34
Pmod JB, pin 10	JB6-7 N	JX1, pin 38	Bank 34, W15	IO_L10N_T1_34
Pmod JC, pin 1	JC0-1 P	JX1, pin 47	Bank 34, N18	IO_L13P_T2_MRCC_34
Pmod JC, pin 2	JC0-1 N	JX1, pin 49	Bank 34, P19	IO_L13N_T2_MRCC_34
Pmod JC, pin 3	JC2-3 P	JX1, pin 48	Bank 34, N20	IO_L14P_T2_SRCC_34
Pmod JC, pin 4	JC2-3 N	JX1, pin 50	Bank 34, P20	IO_L14N_T2_SRCC_34
Pmod JC, pin 7	JC4-5 P	JX1, pin 53	Bank 34, T20	IO_L15P_T2_DQS_34
Pmod JC, pin 8	JC4-5 N	JX1, pin 55	Bank 34, U20	IO_L15N_T2_DQS_34
Pmod JC, pin 9	JC6-7 P	JX1, pin 54	Bank 34, V20	IO_L16P_T2_34
Pmod JC, pin 10	JC6-7 N	JX1, pin 56	Bank 34, W20	IO_L16N_T2_34
Pmod JD, pin 1	JD0-1 P	JX1, pin 67	Bank 34, R16	IO_L19P_T3_34
Pmod JD, pin 2	JD0-1 N	JX1, pin 69	Bank 34,R17	IO_L19N_T3_VREF_34
Pmod JD, pin 3	JD2-3 P	JX1, pin 68	Bank 34, T17	IO_L20P_T3_34
Pmod JD, pin 4	JD2-3 N	JX1, pin 70	Bank 34, R18	IO_L20N_T3_34
Pmod JD, pin 7	JD4-5 P	JX1, pin 73	Bank 34, V17	IO_L21P_T3_DQS_34
Pmod JD, pin 8	JD4-5 N	JX1, pin 75	Bank 34, V18	IO_L21N_T3_DQS_34
Pmod JD, pin 9	JD6-7 P	JX1, pin 74	Bank 34, W18	IO_L22P_T3_34
Pmod JD, pin 10	JD6-7 N	JX1, pin 76	Bank 34, W19	IO_L22N_T3_34
Pmod JK, pin 1	JK0-1 P	JX1, pin 61	Bank 34, Y18	IO_L17P_T2_34
Pmod JK, pin 2	JK0-1 N	JX1, pin 63	Bank 34, Y19	IO_L17N_T2_34
Pmod JK, pin 3	JK2-3 P	JX1, pin 62	Bank 34, V16	IO_L18P_T2_34
Pmod JK, pin 4	JK2-3 N	JX1, pin 64	Bank 34, W16	IO_L18N_T2_34
Pmod JK, pin 7	JK4-5 P	JX1, pin 81	Bank 34, N17	IO_L23P_T3_34
Pmod JK, pin 8	JK4-5 N	JX1, pin 83	Bank 34, P18	IO_L23N_T3_34
Pmod JK, pin 9	JK6-7 P	JX1, pin 82	Bank 34, P15	IO_L24P_T3_34
Pmod JK, pin 10	JK6-7 N	JX1, pin 84	Bank 34, P16	IO_L24N_T3_34

PUDC	PUDC#	JX1, pin 17	Bank 34, U13	IO_L3P_T0_DQS_PUDC_B_34
DONE_LED	FPGA_DONE	JX1, pin 8	Bank 0, R11	DONE_0
CARRIER_SRST#	CARRIER_SRST#	JX1, pin 6	--	--
PWR_EN	PWR_EN	JX1, pin 5	--	--
JTAG_TDO	JTAG_TDO	JX1, pin 3	Bank 0, F6	TDO_0
JTAG_TDI	JTAG_TDI	JX1, pin 4	Bank 0, G6	TDI_0
JTAG_TMS	JTAG_TMS	JX1, pin 2	Bank 0, J6	TMS_0
JTAG_TCK	JTAG_TCK	JX1, pin 1	Bank 0, F9	TCK_0
Pmod_JY, pin 1	JY0-1 P	JX1, pin 87	Bank 13, U7	IO_L11P_T1_SRCC_13
Pmod_JY, pin 2	JY0-1 N	JX1, pin 89	Bank 13, V7	IO_L11N_T1_SRCC_13
Pmod_JY, pin 3	JY2-3 P	JX1, pin 88	Bank 13, T9	IO_L12P_T1_MRCC_13
Pmod_JY, pin 4	JY2-3 N	JX1, pin 90	Bank 13, U10	IO_L12N_T1_MRCC_13
Pmod_JY, pin 7	JY4-5 P	JX1, pin 91	Bank 13, V8	IO_L15P_T2_DQS_13
Pmod_JY, pin 8	JY4-5 N	JX1, pin 93	Bank 13, W8	IO_L15N_T2_DQS_13
Pmod_JY, pin 9	JY6-7 P	JX1, pin 92	Bank 13, T5	IO_L19P_T3_13
Pmod_JY, pin 10	JY6-7 N	JX1, pin 94	Bank 13, U5	IO_L19N_T3_VREF_13
1W_EEPROM, pin 2	1W-EEPROM	JX1, pin 10	Bank 13, T19	IO_25_34

Table 12 – JX2 Connections

Carrier Connection	Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection	Zynq AP SOC Pin
XADC, pin 3	XADC_AD0_P	JX2, pin 17	Bank 35, C20	IO_L1P_T0_AD0P_35
XADC, pin 4	XADC_AD0_N	JX2, pin 19	Bank 35, B20	IO_L1N_T0_AD0N_35
XADC, pin 8	XADC_AD8_P	JX2, pin 18	Bank 35, B19	IO_L1P_T0_AD8P_35
XADC, pin 7	XADC_AD8_N	JX2, pin 20	Bank 35, A20	IO_L1N_T0_AD8N_35
XADC, pin 17	XADC_GIO1	JX2, pin 13	Bank 35, G14	IO_0_35
XADC, pin 18	XADC_GIO0	JX2, pin 47	Bank 35, L16	IO_L11P_T1_SRCC_35
XADC, pin 19	XADC_GIO3	JX2, pin 49	Bank 35, L17	IO_L11N_T1_SRCC_35
XADC, pin 20	XADC_GIO2	JX2, pin 14	Bank 35, J15	IO_25_35
Pmod JE, pin 1	JE0-1 P	JX2, pin 23	Bank 35, E17	IO_L3P_T0_DQS_AD1P_35
Pmod JE, pin 2	JE0-1 N	JX2, pin 25	Bank 35, D18	IO_L3N_T0_DQS_AD1N_35
Pmod JE, pin 3	JE2-3 P	JX2, pin 24	Bank 35, D19	IO_L4P_T0_35
Pmod JE, pin 4	JE2-3 N	JX2, pin 26	Bank 35, D20	IO_L4N_T0_35
Pmod JE, pin 7	JE4-5 P	JX2, pin 29	Bank 35, E18	IO_L5P_T0_AD9P_35
Pmod JE, pin 8	JE4-5 N	JX2, pin 31	Bank 35, E19	IO_L5N_T0_AD9N_35
Pmod JE, pin 9	JE6-7 P	JX2, pin 30	Bank 35, F16	IO_L6P_T0_35
Pmod JE, pin 10	JE6-7 N	JX2, pin 32	Bank 35, F17	IO_L6N_T0_VREF_35
Pmod JF, pin 1	JF0-1 P	JX2, pin 35	Bank 35, L19	IO_L7P_T1_AD2P_35
Pmod JF, pin 2	JF0-1 N	JX2, pin 37	Bank 35, L20	IO_L7N_T1_AD2N_35
Pmod JF, pin 3	JF2-3 P	JX2, pin 36	Bank 35, M19	IO_L8P_T1_AD10P_35
Pmod JF, pin 4	JF2-3 N	JX2, pin 38	Bank 35, M20	IO_L8N_T1_AD10N_35
Pmod JF, pin 7	JF4-5 P	JX2, pin 41	Bank 35, M17	IO_L9P_T1_DQS_AD3P_35
Pmod JF, pin 8	JF4-5 N	JX2, pin 43	Bank 35, M18	IO_L9N_T1_DQS_AD3N_35
Pmod JF, pin 9	JF6-7 P	JX2, pin 42	Bank 35, K19	IO_L10P_T1_AD11P_35
Pmod JF, pin 10	JF6-7 N	JX2, pin 44	Bank 35, J19	IO_L10N_T1_AD11N_35

Pmod JG, pin 1	JG0-1 P	JX2, pin 61	Bank 35, G17	IO_L15P_T2_DQS_AD12P_35
Pmod JG, pin 2	JG0-1 N	JX2, pin 63	Bank 35, G18	IO_L15N_T2_DQS_AD12N_35
Pmod JG, pin 3	JG2-3 P	JX2, pin 62	Bank 35, F19	IO_L16P_T2_35
Pmod JG, pin 4	JG2-3 N	JX2, pin 64	Bank 35, F20	IO_L16N_T2_35
Pmod JG, pin 7	JG4-5 P	JX2, pin 53	Bank 35, H16	IO_L13P_T2_MRCC_35
Pmod JG, pin 8	JG4-5 N	JX2, pin 55	Bank 35, H17	IO_L13N_T2_MRCC_35
Pmod JG, pin 9	JG6-7 P	JX2, pin 54	Bank 35, J18	IO_L14P_T2_AD4P_SRCC_35
Pmod JG, pin 10	JG6-7 N	JX2, pin 56	Bank 35, H18	IO_L14N_T2_AD4N_SRCC_35
Pmod JH, pin 1	JH0-1 P	JX2, pin 73	Bank 35, K14	IO_L20P_T3_AD6P_35
Pmod JH, pin 2	JH0-1 N	JX2, pin 75	Bank 35, J14	IO_L20N_T3_AD6N_35
Pmod JH, pin 3	JH2-3 P	JX2, pin 74	Bank 35, H15	IO_L19P_T3_35
Pmod JH, pin 4	JH2-3 N	JX2, pin 76	Bank 35, G15	IO_L19N_T3_VREF_35
Pmod JH, pin 7	JH4-5 P	JX2, pin 81	Bank 35, N15	IO_L21P_T3_DQS_AD14P_35
Pmod JH, pin 8	JH4-5 N	JX2, pin 83	Bank 35, N16	IO_L21N_T3_DQS_AD14N_35
Pmod JH, pin 9	JH6-7 P	JX2, pin 82	Bank 35,L14	IO_L22P_T3_AD7P_35
Pmod JH, pin 10	JH6-7 N	JX2, pin 84	Bank 35,L15	IO_L22N_T3_AD7N_35
DIP_SW, pin 1	DIP_SW0	JX2, pin 87	Bank 35, M14	IO_L23P_T3_35
DIP_SW, pin 2	DIP_SW1	JX2, pin 89	Bank 35, M15	IO_L23N_T3_35
DIP_SW, pin 3	DIP_SW2	JX2, pin 88	Bank 35, K16	IO_L24P_T3_AD15P_35
DIP_SW, pin 4	DIP_SW3	JX2, pin 90	Bank 35, J16	IO_L24N_T3_AD15N_35
PB, pin 3	PB0	JX2, pin 67	Bank 35, G19	IO_L18P_T2_AD13P_35
PB, pin 3	PB1	JX2, pin 69	Bank 35, G20	IO_L18N_T2_AD13N_35
PB, pin 3	PB2	JX2, pin 68	Bank 35, J20	IO_L17P_T2_AD5P_35
PB, pin 3	PB3	JX2, pin 70	Bank 35, H20	IO_L17N_T2_AD5N_35
BB_CLK_P	BB_CLK_P	JX2, pin 48	Bank 35, K17	IO_L12P_T1_MRCC_35
BB_CLK_EN	BB_CLK_EN	JX2, pin 50	Bank 35, K18	IO_L12N_T1_MRCC_35
PG_CARRIER	PG_CARRIER	JX2, pin, 11	--	N/C
PB_INIT# 2	INIT#	JX2, pin 9	Bank 0, R10	INIT#
VCCIO_EN	VCCIO_EN	JX2, pin 10	Bank 0, L6	PG_1V8
PS_Pmod, pin 1	PMOD_D0	JX2, pin 1	Bank 500, E8	PS_MIO13_500
PS_Pmod, pin 2	PMOD_D1	JX2, pin 2	Bank 500, E9	PS_MIO10_500
PS_Pmod, pin 3	PMOD_D2	JX2, pin 3	Bank 500, C6	PS_MIO11_500
PS_Pmod, pin 4	PMOD_D3	JX2, pin 4	Bank 500, D9	PS_MIO12_500
PS_Pmod, pin 7	PMOD_D4	JX2, pin 5	Bank 500, E6	PS_MIO0_500
PS_Pmod, pin 8	PMOD_D5	JX2, pin 6	Bank 500, B5	PS_MIO9_500
PS_Pmod, pin 9	PMOD_D6	JX2, pin 7	Bank 500, C5	PS_MIO14_500
PS_Pmod, pin 10	PMOD_D7	JX2, pin 8	Bank 500, C8	PS_MIO15_500
Pmod_JZ,pin 1	JZ0-1 P	JX2, pin 93	Bank 13, Y12	IO_L20P_T3_13
Pmod_JZ,pin 2	JZ0-1 N	JX2, pin 95	Bank 13, Y13	IO_L20N_T3_13
Pmod_JZ,pin 3	JZ2-3 P	JX2, pin 94	Bank 13, V11	IO_L21P_T3_DQS_13
Pmod_JZ,pin 4	JZ2-3 N	JX2, pin 96	Bank 13, V10	IO_L21N_T3_DQS_13
Pmod_JZ,pin 7	JZ4-5 P	N/C	--	--
Pmod_JZ,pin 8	JZ4-5 N	JX2, pin 100	Bank 13, V5	IO_L22P_T3_13
Pmod_JZ,pin 9	JZ6-7 P	JX2, pin 97	Bank 13, V6	IO_L22N_T3_13
Pmod_JZ,pin 10	JZ6-7 N	JX2, pin 99	Bank 13, W6	IO_L6N_T0_VREF_13

** Pmod_JY has only 7 connections, thus cannot connect to QSPI or SD interfaces.

2.5.2.2 Layout Routing Guidelines

- The signals for each header follow FMC routing tolerances and guidelines. Each of the P/N pairs have 50Ω single-ended impedance (100Ω differential) with less than 10 mil skew between all P/N pairs on each header.

- There is less than 100 mil length skew across all bits in a bus or byte group, including DQ and DQS pins in each bank.

- The dedicated analog signals, VP_0, VN_0, DXP and DXN are isolated from other noisy signals by putting them at the end of the connector with a GND isolating them from other signals. To minimize noise coupling, the auxiliary/multi-use analog signals, IO_L*P_T1_AD*P/N_* use layer isolation, pair routing and distance separation from other signals. Some of these are shared with DQ byte groups above, in these cases, the DQ routing is more important.

Table 13 – Data Byte Grouping

Byte Group	Zynq Pins	Byte Group	Zynq Pins	Byte Group	Zynq Pins	Byte Group	Zynq Pins
DQ[7:0]	B20 B19 A20 D19 D20 E18 E19 F16	DQ[15:8]	M20 M17 M18 K19 J19 L16 L17 K17	DQ[23:16]	H16 H17 J18 H18 G18 J20 H20 G19	DQ[31:24]	G15 K14 J14 L14 L15 M14 M15 K16

**As chosen by MIG 14.4 for a 7Z010-CLG400 package.*

2.6 Agile Mixed Signaling (AMS) Interface

The XADC header provides analog connectivity for analog reference designs, including AMS daughter cards such as Xilinx's AMS Evaluation Card. Both analog and digital IO can be easily supported for a plug in card.

The pin out has been chosen to provide tightly coupled differential analog pairs on the ribbon cable and to also provide AGND isolation between channels. The plug in cards which will facilitate a number of reference designs have not yet been designed so this pin out must provide a reasonable degree of freedom while also keeping resource requirements as minimal as possible.

The Carrier AMS header is comparable with similar connectors on the Xilinx KC705 and ZC702 boards. Any AMS plug-in cards built for those boards should be compatible with this Carrier as well.

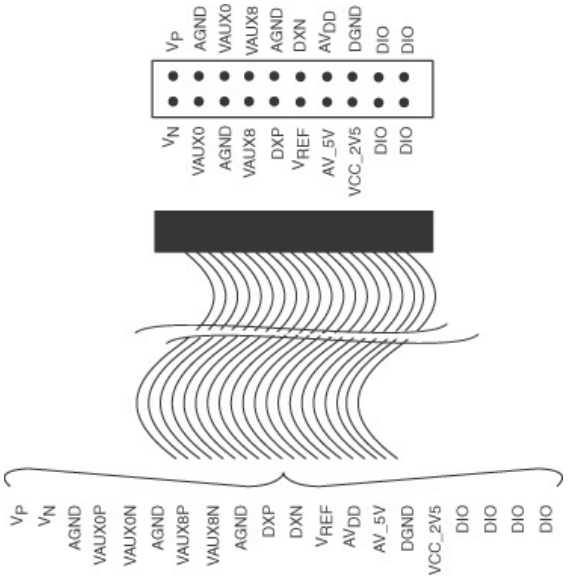

Figure 6 – Analog Header Pin out

The following anti-aliasing filters are used for the XADC inputs:

- VP/VN
- VAUX0P/VAUX0N
- VAUX8P/VAUX8N

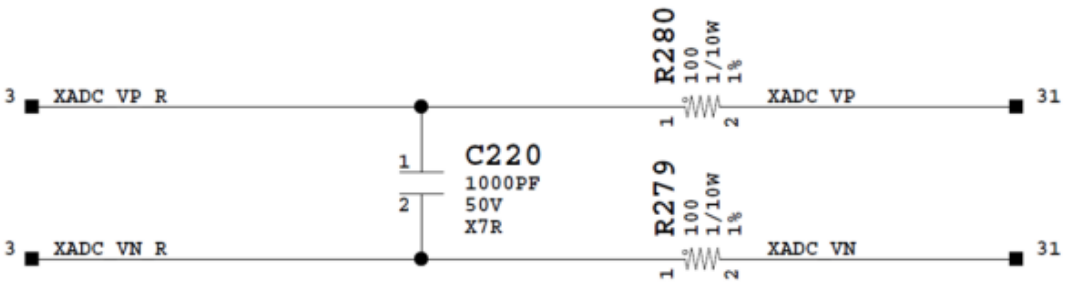

Figure 7 – Anti-Aliasing Filters for XADC Inputs

2.6.1 XADC alternate GPIO function

If the XADC function is not desired, the port can be used for additional GPIO expansion as necessary. However, care must be taken to ensure the appropriate logic voltage levels are observed when using these signals. VCCIO_35 sets the acceptable voltage levels for the XADC_GIOx signals. For AD*_P/N signals must be limited to 1.8V logic levels.

The following signals can be used to perform digital GPIO functionality:

Table 14 - XADC alternate GPIO table

Carrier Connection	Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection	Zynq AP SOC Pin
XADC, pin 3	XADC_AD0_P	JX2, pin 17	Bank 35, C20	IO_L1P_T0_AD0P_35
XADC, pin 4	XADC_AD0_N	JX2, pin 19	Bank 35, B20	IO_L1N_T0_AD0N_35
XADC, pin 8	XADC_AD8_P	JX2, pin 18	Bank 35, B19	IO_L1P_T0_AD8P_35
XADC, pin 7	XADC_AD8_N	JX2, pin 20	Bank 35, A20	IO_L1N_T0_AD8N_35
XADC, pin 17	XADC_GIO1	JX2, pin 13	Bank 35, G14	IO_0_35
XADC, pin 18	XADC_GIO0	JX2, pin 47	Bank 35, L16	IO_L11P_T1_SRCC_35
XADC, pin 19	XADC_GIO3	JX2, pin 49	Bank 35, L17	IO_L11N_T1_SRCC_35
XADC, pin 20	XADC_GIO2	JX2, pin 14	Bank 35, J15	IO_25_35

Table 15 – Analog Header Pin Out

Name	Description	Requirement	XADC Header	Zynq Pin
V_P/V_N	Two pins required. Dedicated pins on the 7 series package. This is the dedicated analog input channel for the ADC(s).	1V peak-to-peak input maximum	1 2	XADC-VN-R : M12 XADC-VP-R : L11
V_{AUX0P}/V_{AUX0N}	Two pins required. Auxiliary analog input channel 0. Two dedicated channels needed for simultaneous sampling applications. Should also support use as IO inputs by disconnection of anti-alias cap see	1V peak-to-peak input maximum	6 3	XADC-AD0N-R : E16 XADC-AD0P-R : F16
V_{AUX8P}/V_{AUX8N}	Two pins required. Auxiliary analog input channel 8. Two dedicated channels needed for simultaneous sampling applications. Should also support use as IO inputs by disconnection of anti-alias cap see	1V peak-to-peak input maximum	7 8	XADC-AD8N-R : D17 XADC-AD8P-R : D16
DXP/DXN	Two pins required. Access to thermal Diode		12 9	XADC-DXN : N12 XADC-DXP : N11
AGND	Three pins required. Analog ground reference GNDADC. Analog channel isolation		4 5 10	
VCCADC	One pin. This is the analog 1.8V supply for XADC.	1.8V ±5% @150mA max	14	
V_{REF}	One pin. This is the 1.25V reference from the board.	1.25V ±0.2% 50ppm/ºC @5mA max	11	
AV_5V	Filtered 5V supply from board.	5V ±5% @150mA max	13	
GPIO	General Purpose I/O	Voltage set by Vadj	G0: 18 G1: 17 G2: 20 G3: 19	H15 R15 K15 J15
Vadj	Adjustable Voltage	1.8V, 2.5V, 3.3V		

2.7 JTAG Configuration

The Carrier provides a traditional Platform Cable JTAG connector for use with Xilinx Platform Cables and Digilent JTAG HS1 or HS2 Programming Cables. When a MicroZed is plugged onto the Carrier, the Carrier's JTAG connector MUST be used. The JTAG connector on-board the MicroZed SOM will no longer function.

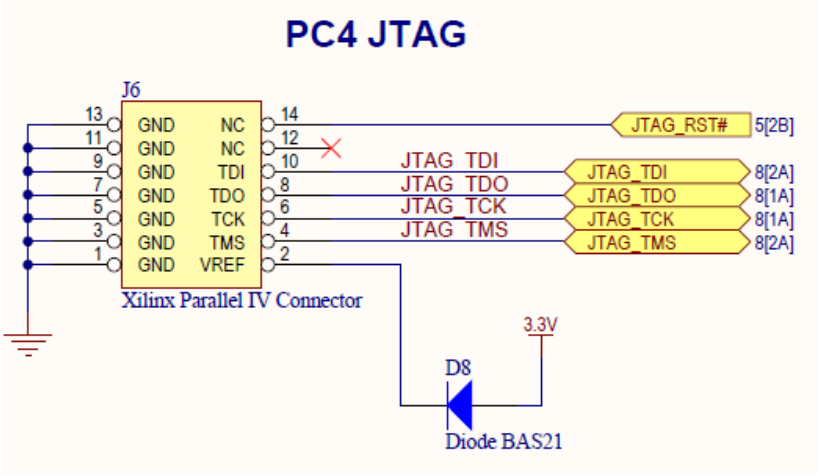

Figure 8 – JTAG Connections

The Carrier has a 3-pin jumper connecting to PUDC_B. Default is???

Table 16 – PUDC_B Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection	Zynq AP SOC Pin
PUDC#	JX1, pin 17	Bank 34, U13	IO_L3P_T0_DQS_PUDC_B_34

A blue DONE LED is connected to Zynq through the MicroHeader. When the PL is properly configured, the DONE LED will light.

Table 17 – Done Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection	Zynq AP SOC Pin
FPGA_DONE	JX1, pin 8	Bank 0, R11	DONE_0

INIT_B and POR are connected to pushbuttons on the Carrier.

Table 18 – Configuration Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SOC Connection	Zynq AP SOC Pin
INIT#	JX2, pin 9	Bank 0, R10	INIT_B_0
VCCIO_EN	JX2, pin 10	None	None

2.8 Power

2.8.1 Power Input

The board input voltage is through a 2.1mm/5.5mm inner/outer, center positive barrel jack, CON2. The input voltage range is from 5V to 12 volts. The current rating of the power supply is determined by the total expected power consumption of the project. The default power supply sent by Avnet is a 5V, 2 Ampere power supply for general low power I/O applications and XADC header use.

Additionally, there are 50 I/O on Bank 34, and as many as 66 I/O on Banks 35/13. At 16mA drivers and 66 I/O equates to a max current of 1.056A @ 3.3V. The PMOD power connections are capable of sourcing 3.3V at 100mA each.

The precise current demand is based on the end-use I/O requirements and therefore the application will determine the minimum current a power supply must source. As shipped from Avnet, a 5V, 2 Amp or larger power supply is provided in the kit.

- Barrel Jack Input:
  - 5V ≥ 2A Barrel Jack, 2.1mm inner/5.5mm outer diameter center positive while using XADC.

- On Board:
  - Filtered 5V to A5V:
    - For MicroZed Module & XADC.
  - >85% high-efficiency regulators for 1.8V/2.5V/3.3V @ 2.3A
    - For Module VCC_{IO} Bank_34
  - >85% high-efficiency regulators for 1.8V/2.5V/3.3V @ 2.85A
    - For Module VCC_{IO} Bank_35 and Bank 13 (7Z020 only)
  - Low noise LDO 1.8V @ 0.15A supply for XADC

2.8.2 Voltage Regulators

The following table lists the power solution for the IO Carrier Card. Two rails are independent and adjustable supplying power to the Zynq PL I/O banks and connected Pmods™. VCCio_35 drives banks 35 and 13 (if 7Z020 is populated on MicroZed) as well as 5 Pmod™ connectors.

The table below shows the minimum required voltage rails, currents, and tolerances.

Table 19 – Voltage Rails w/ Current Estimates

Voltage (V)	7Z010 Current	7Z020 Current	Tolerance	IC	Notes
Vin (MicroZed Module)	5W	6.5W	5.00%	N/A	Filtered from Vin, J4.3
Vadj (VCCio_34) – 1.8V, 2.5V or 3.3V	2.3A @ 3.3V	2.3A @ 3.3V	5.00%	REG3, MAX15066	Pmods + VCCio Banks, TP8
Vadj (VCCio_35) – 1.8V, 2.5V or 3.3V	<2.0A @ 3.3V	2.85A @ 3.3V	5.00%	REG4, MAX15066	Pmods + VCCio Banks, TP9
1.8 (analog/Vccadc)	150 mA	150 mA	5.00%	REG1, MAX8891-18	Filtered from Vin, TP6
1.25V (analog/Vref)	50 mA	50 mA	0.2%	REG2, MAX6037A-12	Filtered from Vin, TP7
3.3V Main	490 mA	500 mA	5.00%	REG5, MAX17501EATB+	Filtered from Vin, TP10
5.0V (analog/AMS)	0.15A	0.15A	5.00%	N/A	Filtered from Vin, Top of C36

2.8.3 Sequencing

- PWR_EN signal, active high, JX1.5, allows the carrier to turn on or off the MicroZed power supplies. R81 and C93 have been placed to facilitate the timing of this signal during power off conditions. This signal should not be de-asserted until VCCIO_EN is de-asserted. In the carrier off condition (power plug removed or power switch turned off), this signal is driven low by the carrier board.

- VCCIO_EN signal, active high, JX2.10, originates on the microZed and is the output of the 1.8V regulator, PG_1V8. This signal enables the carrier's 3.3V supply, which in turn enables both VCCIO_34 and VCCIO_13/35. When the carrier is turned off (power switch turned off or power plug removed) or the MicroZed's PG_1V8 signal is de-asserted VCCI_EN is driven low, which turns off the IOCC and the MicroZed.

- PG_CARRIER signal, active high, JX2.11, is pulled up by MicroZed's +3.3V PG_MODULE signal. This signal is pulled low by the carrier board or the MicroZed when either board's power circuitry is not 'Good' yet.

- The following diagram illustrates the power supply sequencing on power up. Note Vin and PWR_Enable can come up simultaneously, but shown staggered as PWR_Enable can come up later.

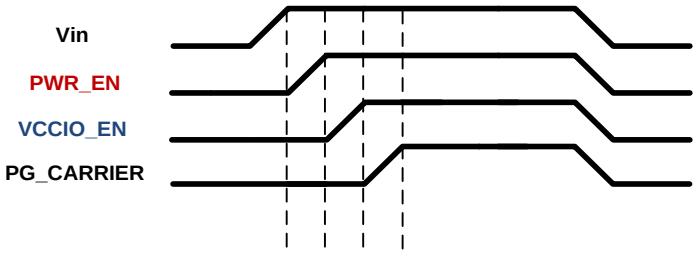

Figure 9 – Power Sequencing

The 3.3V regulator on the carrier is enabled by the VCCIO_EN signal which in truns enables the VCCIO regulators. The VCCIO regulators are sequenced in series and cannot be enabled until Zynq's core power is valid. The PG_CARRIER (on IOCC) and PG_MODULE (on MicroZed) signals are wired OR and tied to the Zynq Power On Reset signal. When the power supplies are valid on both the SOM and carrier, the PG signal de-asserts the Zynq POR signal.

2.8.4 Bypassing/Decoupling

The IOCC follows the recommended decoupling techniques per each manufacturer's datasheet.

2.8.5 System Power Good LED

A green status LED indicates when PG_CARRIER and/or PG_MODULE is good.

2.9 Jumpers, configuration and test points:

The below table is a quick reference to all of the jumpers, configuration settings and test points on the IOCC. For detailed information, refer to the appropriate sections in this document.

Reference Designator	Name	Default	Notes:
J1	PUDC#	Short 1-2 (disabled)	Active low.
J2	JTAG	Populated	Zynq JTAG interface.
J3	VBAT	Not Populated	JX1 pin 7. Zynq pin F11. +1.8V for FPGA battery support.
J4	Fan Header	Not Populated	Attached to Vin
J5	VCCIO_EN	Not Populated	Used to test the on-board power supplies without a MicroZed inserted.
J6	PG_CARRIER	Not Populated	Used to test the on-board power supplies without a MicroZed inserted.
DIP_SW0-3	DIP_SWx	In low position	4 user slide switches to the Zynq PL fabric. Pulled low. Active when high.
SW2	POR#	Open	Active low Power On Reset signal. See section 2.3.2.
SW3	INIT#	Open	Active low initialization signal. Rarely used. See section 2.3.1.
SW4	CARRIER_SRST#	Open	Active low FPGA PS reset. Interfaced with JTAG J2. See section 2.3.3.
TP1	CARRIER_SRST	N/A	Signal monitor test point
TP2-5	GND	N/A	Power supply ground
TP6	A1V8	N/A	Analog +1.8V test point
TP7	VREF_1V25	N/A	+1.25V test point
TP8	VCCIO_34	N/A	VCCIO_34 test point
TP9	VCCIO_35	N/A	VCCIO_35 test point
TP10	3V3	N/A	+3.3V test point
CON3	VCCIO_34	Short 1-2	+3.3V setting for VCCIO_34
CON4	VCCIO_35	Short 1-2	+3.3V setting for VCCIO_35
BTN1-4	BTNx	Open	4 user input pushbuttons to the Zynq PL fabric. Pulled low, active high via VCCIO_35 voltage setting when depressed.

Table 20 - settings

3 Mechanical

3.1 Dimensions:

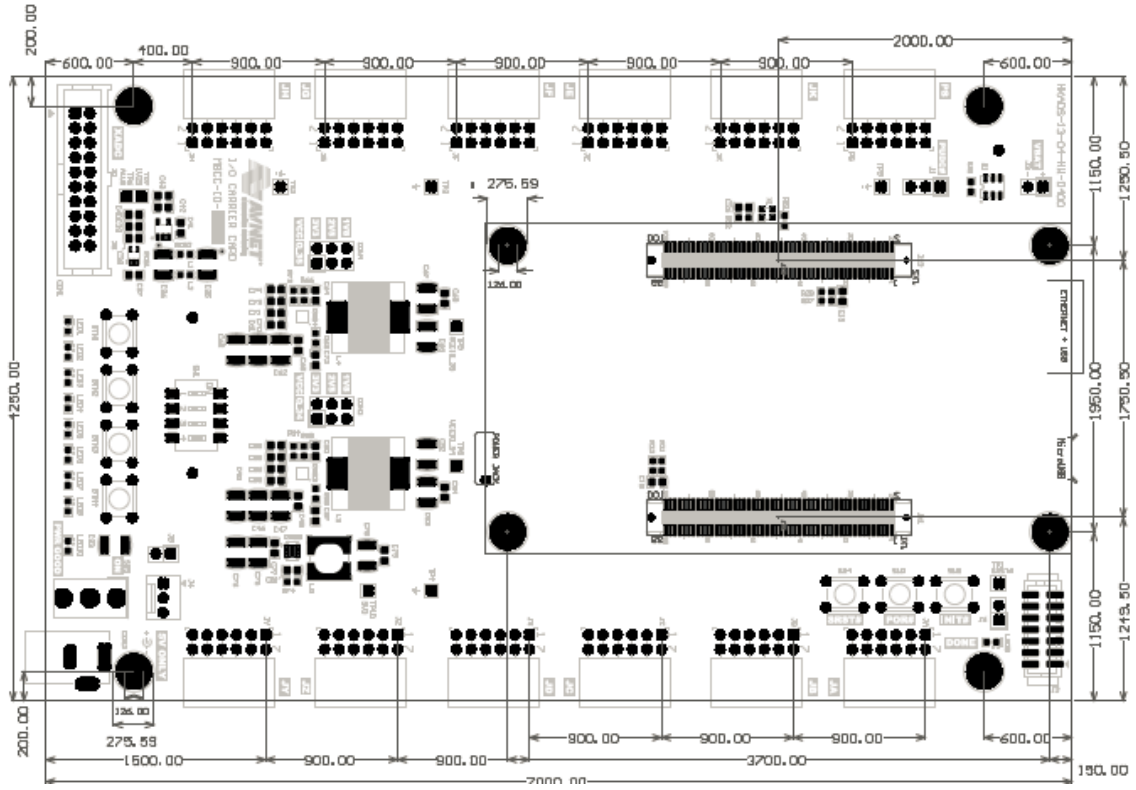

Figure 10: IOCC Horizontal Mechanical Dimensions (mils)

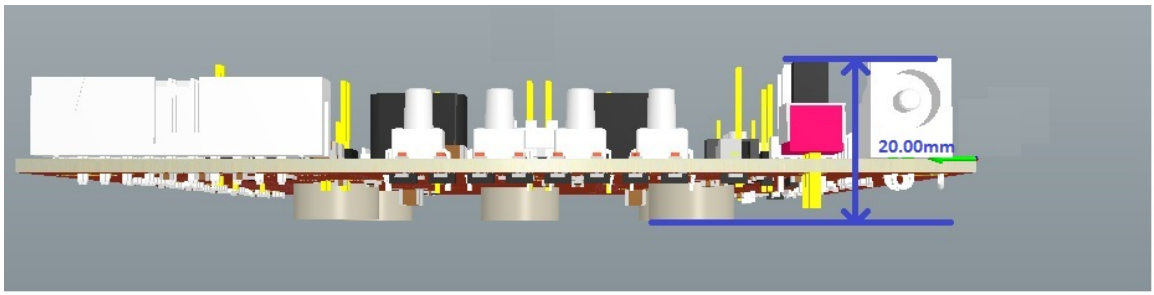

Figure 11 - Total height from Bumper to Switch top – 20.00 mm

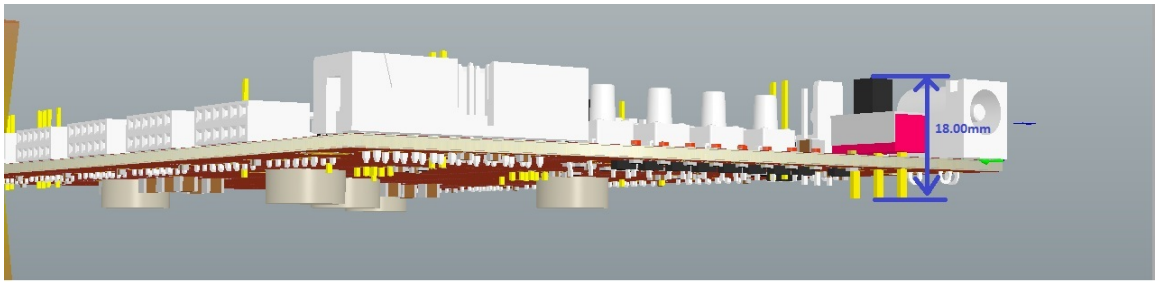

Figure 12 - Switch Height - no bumpers – 18.00 mm

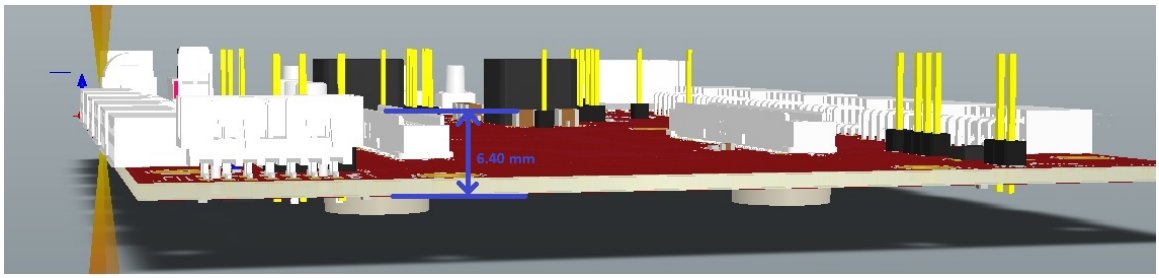

Figure 13 - bottom of PCB to top of JX.x connector – 6.40 mm

3.2 Weight:

The weight of the IOCC with rubber feet and all jumpers populated is 110 grams/3.8801 oZ.

4 Revision History

Rev date	Rev #	Reason for change
7 Feb 2014	1.0	Updated images & TOC.
6 Mar 2014	1.1	Updated images, dimensions & TOC.
21 Apr 2014	1.2	Updated PMOD JF section.
20 Aug 2014	1.3	Corrected errors and formatted Tables 6, 12, 13, and 15