Revision C Changes:
1) Add Silkscreen Logos - CE, RoHS and Copper Part Number on board.
2) Reduce R34, 35, (40), 42 from 100K to 1K.
3) Add pull-down resistors to R34, 35, (40), 42 - Values 2.2K - 5.00K.
4) Fuse (PTC) recommendation note for R50, 12V input.
5) Connect U7.B to D8.B.
6) Connect U7.C to D8.C.
7) Revised wire: Connect JX2.10 to U21.4.
8) Change 4.75K resistor to 4.99K.
9) Add rubber feet to BOM - TBD.
10) Added staple points (vias) for J2.
MicroZed 7010

Block Diagram

Avnet Engineering Services

Title: Block Diagram

Size: Rev:

Document Number:

Date: Sheet of 10/25/2013 2

C

MicroZed 7010

ZYNQ XC7Z010-CLG400

Dedicated

PS

PL

Microheader
Layout Note:
Use fly-by routing and termination for DDR3 control signals. Resistors should be placed past the test memory IC & a few inches to the device as possible.

Layout Note:
DDR3 trace lengths must include zero pin spacing & flyby. See schematic & layout guidelines.

Layout Note:
DDR3 target trace impedances are as follows: Single Ended Signals = 48 ohms Differential Signals = 50 ohms
Device Mode = 10K
Host/OTG Mode = 1K

Component Notes:
- Default these components are placed, not to exceed 500mA handling, can be a selectable PTC value, pending customer requirements.
- Generic PTCs can be placed if greater than +5.0 Vin

Design Note:
- USB is a 2432 footprint, Generic PTCs can be placed, not to exceed 500mA handling, can be a selectable PTC value, pending customer requirements.

Layout Note:
- USB VBUS_OTG net must be 500uA or more capable.
- USB_VBUS_UART net must be 1mA or more capable.

Layout Note:
- USB differential signal impedance target is 50 ohms.
- USB_A differential signal impedance target is 50 ohms.