PicoZed 7015/7030 SOM

Revision E
128 Mb QSPI

1 GB DDR3

4 GB or 8 GB eMMC

JX1 Micro Header
50/58 User I/O
(7Z010/7Z015-20-30)

JX2 Micro Header
50/57 User I/O
(7Z010/7Z015-20-30)

XC7Z010/20-1
CLG400

XC7Z015-1
CLG485

XC7Z030-1
SBG485

Processing System

Programmable Logic

OSC @ 33.33 MHz

USB 2.0
ULPI PHY

Ethernet
PHY

JX3 Micro Header
Ethernet / USB 2.0 OTG
10/20 User I/O
(7Z020/7Z015-30)
4 GTP/GTX Ports
(7Z015/7Z030)
Zynq PS DDR - Bank 502

BANK 502

DDR3

DDR3 Termination Supply

Layout Note:
- DDR3 trace lengths must include Zynq package footprint to meet DDR3 timing requirements.
- Use P16 by routing and termination for DDR3 control signals.
- Resistor values should be matched as close to the device as possible.

Layout Note:
- DDR3 target trace impedances are as follows:
  - Single Ended Signals = 40ohms
  - Differential Signals = 160ohms

NOTE:
- RE349T requires a pull-down resistor through FPGA to ensure DDR3 is low during power-up.
- USB board and power supply must be isolated.
WARNING!!!

Bank 34 and Bank 35 are High Performance banks (7030 only) and will only accept 1.8V level signals. Failure to limit Bank 34 and 35 to 1.8V signals can damage the Zynq 7030 AP SoC.
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I/O POWER

CORE POWER

GTX POWER

DIGITAL GND

VCCINT

VCC_BRAM

VCC_AUX

VCCO_13

VCCO_34

VCCO_35

BANK 0

VCCPINT

VCC_PAUX

VCCO_DDR

VCCO_MIO0

VCC_MIO1

VCC_PLL

AVNET Avnet Engineering Services
PicoZed 7035/7030 SOM
SC4-072509
ID: PIC15001
Date: 12/18/2017
Sheet: 1
Variant: 01
Doc Num: 10 - DEVICE POWER.SchDoc B
Project Name: SCH-PZ2SOM
Time: 11:06:39 AM
BOM: 01
Revision History

Rev B
1) Updated Block Diagram
2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
3) Added RC time constant to ETHERNET RESET
4) DDR3L/DDR3 option note added
5) Renamed 1.5V and DDR3_0V75 power nets
6) Changed U4.2 connection from 1.8V to 3.3V
7) Changed JX1/JX2 connections to Zynq Bank 34/35 Clock Capable Pins

Rev C
1) U18, U19, JT1, JT5, and JT6 have been removed
2) U4, U15, and U17 part numbers changed
3) Moved C84, C96, C101, C107, C111, C114, C134, C140, C142, C15, C161, C183, R86, RP2, L3, L4, L5, L6, L7, L8, and U16 away from FPGA to allow for heatsink clearance
4) JT8 and JT9 added to allow Boot Mode to be hard wired with 0 Ohm Jumpers
5) JT6 Replaced with 4.99K Pulldown resistor

Rev D
1) Connected U17 Pin B3 to GND
2) Added Voltage Divider (R52, R96) and filter cap (C195) to U4 "VRI" pin
3) Added C199 and C200 to U15 Pin 3/5 (DDR3_VTT)
4) Added C196 to U15 Pin 2 (PVcc)
5) Changed C42 to 0.1uF Cap
6) Changed C39 to 4.7uF Cap

Rev E
1) Added shared circuit MIO47 to JX3 and ETHERNET RESET
2) Added RC time constant to ETHERNET RESET
3) Added DDR3L/DDR3 option note added
4) Renamed 1.5V and DDR3_0V75 power nets
5) Changed U4.2 connection from 1.8V to 3.3V
6) Changed JX1/JX2 connections to Zynq Bank 34/35 Clock Capable Pins