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**PicoZed - Rev B**

9/15/2014

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Zynq PS DDR - Bank 502

Layout Note:
DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.

Layout Note:

DD5 should be routed and terminated for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.

Layout Note:

DDR3 trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms

Layout Note:

Note: PIU6 does not support the pull-down resistor on the
DDR3 DQ[23..16] ties. Please refer to the pull-down
resistor guidelines.
All RSVD_MGT* signals are reserved for devices with MGTs.

*All RSVD_MGT* signals are RESERVED for devices with MGTs.
Revision Notes:
02 Sep 2014
1) Multiplexed JX2 MIO signals with EMMC
2) Removed Push Button footprint
3) Incorporated ETHERNET RESET circuit
4) Added bulk cap to AVDD18
5) Added GND Testpoints
15 Sep 2014
1) Updated BOOT MODE table

Mechanicals:

PCB Mounting Holes

GND Test Points

Fansink Mounting Holes