Zynq PS MIO - Bank 500

Embedded eMMC: 2GB, 4GB, 8GB

Boot Mode Select

CAS-CASCADE-JTAG - DEFAULT MODE
Revision Notes:

PicoZed Revision B1:
1) Multiplexed JX2 MIO signals with EMMC
2) Removed Push Button Footprint
3) Incorporated ETHERNET RESET circuit
4) Added bulk cap to AVDD18
5) Added GND Testpoints

PicoZed Revision B2:
1) Updated BOOT-MODE table

PicoZed Revision C:
1) Updated Block Diagram
2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
3) Added RC time constant to ETHERNET RESET
4) DDR3L/DDR3 Option Added
5) Modified resistor divider value on PG_1V8
6) Changed DDR3 Termination Regulator VLDOIN from 1.8V to 3.3V

PicoZed Revision C (Errata):
1) R71: Changed to 4.99K
2) R192: Changed to 0.1uF

Mechanicals:

PCB Mounting Holes

GND Test Points

Fansink Mounting Holes