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128 Mb QSPI
1 GB DDR3
4 GB eMMC *
OSC @ 33.33 MHz

XC7Z015/30-1SBG485
Processing System

USB 2.0 ULPI PHY
Ethernet PHY
12 MIO
8 MIO *

JX3 Connector
JX3 Connector
JX3 Connector
JX2 Connector

JX3 Micro Header (Bank 13)
20/20 User I/O

JX1 Micro Header (Bank 13)
8/58 User I/O

JX1 Micro Header
50/58 User I/O

Programmable Logic

GTP/GTX

JX2 Micro Header (Bank 13)
7/57 User I/O

JX2 Micro Header
50/57 User I/O

JX3 Connector

* eMMC and MIO Interface Shared on JX2
Layout Note: Zynq package flight times. See USB3 and Layout Guidelines.

Layout Note: DDR3 trace lengths must include Zynq package flight times. See USB3 and Layout Guidelines.

Layout Note: DDR3 target trace impedances are as follows: Single-Ended Signals = 40 ohms. Differential Signals = 90 ohms.

Default Pins 2-3, 1K ohm resistors.

NOTE: Resistor is 1K resistor for PS to maintain logic high in configuration. See USB3 signal.
WARNING!!!
Bank 34 and Bank 35 are High Performance banks (7030 only) and will only accept 1.8V level signals. Failure to limit Bank 34 and 35 to 1.8V signals can damage the Zynq 7030 AP SoC.
WARNING!!!
Bank 34 and Bank 35 are High Performance banks (7030 only) and will only accept 1.8V level signals. Failure to limit Bank 34 and 35 to 1.8V signals can damage the Zynq 7030 AP SoC.
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11 - POWER, RESET.SchDoc

Avnet Engineering Services

PicoZed 7015/7030

of
Revision History
Rev B
Original release

Rev C
1) Updated Block Diagram
2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
3) Added RC time constant to ETHERNET RESET
4) DDR3L/DDR3 option note added
5) Renamed 1.5V and DDR3_0V75 power nets
6) Changed U4.2 connection from 1.8V to 3.3V
7) Changed JX1/JX2 connections to Zynq Bank 34/35 Clock Capable Pins

Mechanicals:

PCB Mounting Holes

GND Test Points

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