Subject: PicoZed SOM PCB revision is moving from Rev-C to Rev-E

Products Affected: This PCN affects the part numbers listed below.

AES-Z7PZ-7Z010-SOM-G    AES-Z7PZ-7Z010-SOM-I-G
AES-Z7PZ-7Z020-SOM-G    AES-Z7PZ-7Z020-SOM-I-G
AES-Z7PZ-7Z015-SOM-G    AES-Z7PZ-7Z015-SOM-I-G
AES-Z7PZ-7Z030-SOM-G    AES-Z7PZ-7Z030-SOM-I-G

Change Description:

Removed Muxes (U1 & U2) to improve eMMC performance: The Muxes were replaced by resistor jumper that are by default set to position 1-2 connecting PS_MIO10 though 15 to the eMMC control signals as shown below.

With these jumpers in their default position the MIO10 through MIO15 pins on the connector JX2 are not usable. Moving the resistor jumpers from their default position to 2-3 will restore access to these I/O pins but will disable the eMMC mass storage device.

<table>
<thead>
<tr>
<th>EMCCMIO10 (pad 1)</th>
<th>PS_MIO10 (pad 2)</th>
<th>MIO10 (pad 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMCCMIO11 (pad 1)</td>
<td>PS_MIO11 (pad 2)</td>
<td>MIO11 (pad 3)</td>
</tr>
<tr>
<td>EMCCMIO12 (pad 1)</td>
<td>PS_MIO12 (pad 2)</td>
<td>MIO12 (pad 3)</td>
</tr>
<tr>
<td>EMCCMIO13 (pad 1)</td>
<td>PS_MIO13 (pad 2)</td>
<td>MIO13 (pad 3)</td>
</tr>
<tr>
<td>EMCCMIO14 (pad 1)</td>
<td>PS_MIO14 (pad 2)</td>
<td>MIO14 (pad 3)</td>
</tr>
<tr>
<td>EMCCMIO15 (pad 1)</td>
<td>PS_MIO15 (pad 2)</td>
<td>MIO15 (pad 3)</td>
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Allow for clip-on Heat Sink: Moved Passive devices away from the Zynq device providing the clearance necessary for supporting common clips.

DDR3 termination regulator, U15 replaced with NCP51400: This change allowed for a reduction in the BOM cost.

BOM Changes:

a) Passive and interconnect part selection altered to conform to the current supply chain to reduce lead-times.
b) QSPI FLASH, U6, Changed preferred source to Micron MT25QL128ABA8E12-0SIT and retaining Spansion as an alternate
c) eMMC, U3, Upgraded from v4.41 4GB to v5.0 8GB “MTFC8GAKAJCN-4M IT” to improve availability and enhance the feature.
d) Depopulate C3, C5 & C6; This change was required to support Host or OTG mode of the Microchip USB3320.

Reason for Change:

The removal of the Mux devices was done to support the 50MHz maximum clock rate to the eMMC device.
More Information

The changes made beyond the mux removal were made to improve the usability and supply chain for the board.

Note: Rev-D was never built so the transition from rev-C to rev-E is a single step.

Care was taken to insure that in its default state and with the exception of MIO10 – MIO15 the PicoZed Rev-E board will operate just as the PicoZed Rev-C does so there is no need for most customers to modify their designs.

When the base part numbers listed above are ordered Avnet reserves the right to ship either rev-C or rev-E depending on inventory available, however customers can also stipulate a version by adding the revision to the part number (AES-Z7PZ-7Z020-SOM-G/REV-E). There are no plans to build PicoZed Rev-C after December 2017 but there will be inventory in stock for several months during the transition.

Customers with PicoZed SOMs in products are encouraged to qualify the Rev-E boards as quickly as possible to avoid sourcing issues in the future. If for any reason the Rev-E board can’t be qualified Avnet can continue to build the rev-C boards but an MOQ may be required.

The latest documentation, including schematics, can be found on the product page.

http://picozed.org/product/picozed

For any questions regarding this PCN please use the PicoZed Hardware Design Forum.